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HEINZ NIXDORF INSTITUT
UNIVERSITÄT PADERBORN

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Direkt-detektierenden Wake-up-Empfänger mit geringer Leistungsaufnahme bei 2,44 GHz für drahtlose Sensornetzwerke

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Abstract

This work demonstrates the design, implementations and measurements of a 2.44 GHz direct-detection Wake-up Receiver (WuRx) based on Surface Acoustic Wave (SAW) correlator. The choice of direct-detection architecture for Radio Frequency (RF) radios allows for low-power dissipation. However, it suffers from high sensitivity to co-channel interference and poor receiver sensitivity, which reduce the communication performance and reliability. To improve the receiver sensitivity, the baseband bandwidth is reduced by means of an innovative Narrowband Correlator (NBC) in conjunction with Pulse Position Modulation (PPM) communication scheme, which allows for scalable receiver sensitivity versus data-rate. Additionally, to improve co-channel interference robustness, the receiver architecture uses 2.44 GHz 13-bits Binary-phase Shift Keying (BPSK) Barker-coded SAW correlator, which is fabricated on Lithium Niobate ($LiNbO_3$) substrate. It functions as a passive detection stage to the input RF signal and provides a mechanism for interferer suppression. The receiver is designed in CMOS TSMC65nm technology and achieves a power dissipation of 142 µW from a 1.2 V supply source, and a receiver sensitivity of −44 dBm and −50 dBm at a data-rate of 2 Mbps and 600 kbps respectively.

The WuRx can be used in Wireless Sensor Networks (WSNs) to reduce the power dissipation of nodes and extend their operating lifetime. WSN nodes are often powered by batteries, which makes the power dissipation the major challenge in the design of WSN. If each WSN node contains an integrated WuRx, which is always-on and listening for a wake-up signal from other nodes or the base station, the communication scheme becomes asynchronous, real-time and on-demand. Additionally, the WuRx with improved co-channel interference robustness reduces false positive wake-up signals to the WSN nodes, and provides a reliable communication scheme for the WSN in coexistence with other wireless systems.

Zusammenfassung

In dieser Arbeit wird der Entwurf, die Implementierung und die messtechnische Charakterisierung eines direkt-detektierenden Wake-up-Empfängers (engl. wake-up receiver, WuRx) bei 2.44 GHz auf Basis eines Surface-Acoustic-Wave (SAW) Korrelators untersucht. Die Wahl einer Direktdetektionsarchitektur für Hochfrequenz (HF)-Funkgeräte erfolgt durch die Bedingung einer geringen Leistungsaufnahme. Allerdings leidet diese Architektur unter einer hohen Empfindlichkeit für Ko-Kanal-Interferenz, was die Kommunikationsleistung und -zuverlässigkeit des Systems verringern. Um die Empfängerempfindlichkeit zu verbessern, wird die Bandbreite des Basisbands durch einen innovativen Schmalband Korrelator (engl. narrow band correlator, NBC) in Verbindung mit Pulse-Position-Modulation (PPM) reduziert, was eine skalierbare Empfängerempfindlichkeit gegenüber der Datenrate ermöglicht. Um die Robustheit gegenüber Gleichkanalstörungen zu verbessern, verwendet die Empfängerarchitektur einen 2.44 GHz Barker-Korrelator mit 13 Bits und einen mit binärer Phasenumtastung (BPSK) kodierten SAW-Korrelator, der auf einem Lithium-Niobat ($LiNbO3$)-Substrat hergestellt wird. Er fungiert als passive Detektionsstufe für das RF-Eingangssignal und bietet einen Mechanismus zur Unterdrückung von Störsignalen. Der Empfänger wurde in TSMC65nm CMOS-Technologie entwickelt und erreicht eine Leistungaufnahme von nur 142 µW bei einer Versorgungsspannung von1.2 V sowie eine Empfängersensitivität von −44 dBm bei einer Datenrate von 2 Mbps bzw. −50 dBm bei einer Datenrate 600 kbps.

Der WuRx kann in drahtlosen Sensornetzwerken (engl. wireless sensor networks, WSNs) eingesetzt werden, um die Leistungsaufnahme von Netzwerkknoten zu reduzieren und ihre Lebensdauer zu verlängern. WSN-Knoten werden häufig energetisch von Batterien versorgt, was die Leistungsaufnahme zur größten Herausforderung bei der Entwicklung von WSN macht. Wenn jeder WSN-Knoten einen integrierten WuRx enthält, der immer eingeschaltet ist und auf ein Wecksignal von anderen Knoten oder der Basisstation wartet, wird das Kommunikationsschema asynchron, in Echtzeit und anfragenbasiert. Außerdem reduziert der WuRx mit verbesserter Ko-Kanal-Interferenz-Robustheit die Anzahl falschpositiver Wecksignale für die WSN-Knoten und bietet ein zuverlässiges Kommunikationsschema für das WSN in Koexistenz mit benachbarten Drahtlossystemen.

Low-power Direct-detection Wake-up Receiver at 2.44 GHz for Wireless Sensor Networks

Contents

1 Introduction

Computer networks have become an essential part in several application fields such as education, transportation, business and industry. They are capable of carrying information and making it available to end-users regardless of their physical locations [1]. The improvement in wireless communication technologies contributes significantly to the wide spread use of Wireless Sensor Networks (WSNs). The WSN is a type of computer network that is distributed over a wide geographical area. It is composed of a large number of autonomous sensor nodes that are connected to each other or to the base station via wireless communication links. The WSN has unique design considerations that differentiate it from other types of computer networks, such as low-power dissipation, scalability, physically small sensor nodes and low node-cost [2]. In wireless communication systems, the communication process dissipates a considerable amount of power, which degrades significantly the network operating lifetime and communication reliability. Hence, the power dissipation becomes a major design challenge given that the sensor nodes are operating with limited power budget. Typically, batteries are used to power-up the sensor nodes, or in the optimal case, an energy harvesting technique is utilized, providing unlimited operating lifetime. In the case of a battery-based WSN, periodic battery replacement or charging is required. In some WSN applications, e.g. where the sensor nodes are located in harsh environment, battery replacement or charging is infeasible. In such scenarios, the sensor node is simply discarded once its energy source is depleted. The sensor node lifetime design constraint varies gradually depending on its application scope, e.g. if the sensor node is used in weather monitoring, then it has to work for the longest possible operating period, while sensor node that is used in pipelines technical inspection (water or oil pipelines) requires few hours of operating lifetime [2].

In this chapter, an introduction about the WSNs and their design challenges are presented, followed by the WSN applications scope. A comparison overview of common WSN power reduction techniques is given, addressing their working principle. The chapter ends with the thesis main contributions and outline.

1.1 Wireless Sensor Network and its Applications

Figure 1.1 shows a WSN distributed into two different geographical areas. Both sensor fields are connected to the base station, which is connected to the internet. The WSN nodes are able to detect signals from the physical environment and connect them to the internet, making it possible to perform a sequence of operations on the gathered information including processing, storing and taking actions [1], [2]. The WSN nodes perform simple to complex tasks. For example, one WSN node senses temperature or humidity, and another node makes acoustic or magnetic measurements. The WSN consists of a certain number of sensor nodes that are distributed over an area with different wireless link distances, therefore it is not practical to power-up each node with a constant energy source, but batteries are usually used. Beside the low-power design constraint, nodes have to be small and exhibit high level of system integration, providing flexibility in installation and

deployment. Self-management of the WSN and sensor nodes is another design challenge, where they adapt their operating parameters, such as resources allocation, frequency and data-rate accordingly. The WSN security is an additional important design target, where the nodes have to be immune against security threats such as Denial-of-Service (DoS) attacks [2], [3]. Detailed WSN design considerations are given in Chapter 3.

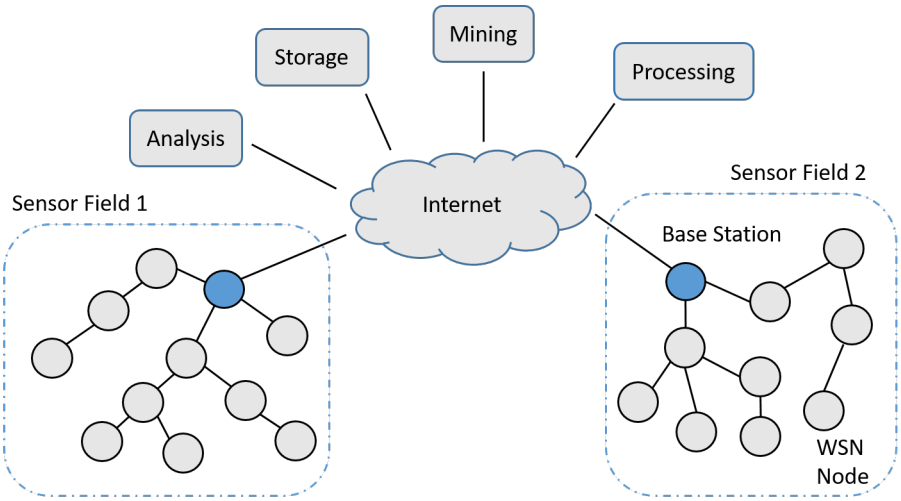


Figure 1.1: *A Wireless Sensor Network (WSN) [2]*

The communication synchronization between the base station and the WSN nodes has a significant impact on the node's power dissipation. The synchronization is classified into three categories. The first is the purely synchronous communication scheme, in which a precise synchronization and a specific communication time-slots agreements between the base station and the WSN nodes are set up, which results in a reliable communication scheme, but dissipates a large amount of power. Another approach of communication synchronization is the pseudo-asynchronous (or duty-cycled scheme), where the WSN nodes has a periodic operation timing, trading-off the power dissipation with information and data-latency. The last communication scheme is the purely asynchronous. One variant of this communication scheme requires integrating of an extra hardware into each WSN node, which operates as a low-power Wake-up Receiver (WuRx), making the communication between each node and the base station or other WSN node asynchronous, real-time, and on-demand [4]. With this communication scheme, the energy efficiency, reliability and failure-rate of WSN nodes are improved, since they are only activated when a wake-up-signal is received. In addition to low-power dissipation, the WuRx design must be robust to noise and co-channel interference in order to operate reliably in parallel to other wireless systems.

The unique WSN node characteristics such as low-power dissipation, low-cost, high level of integration, small size and self-management enable the WSN to have a wide application scope. Common WSN application fields are:

- **Health care:** the WSN is applied to the health care services. WSNs can be used to monitor patients with diseases such as heart problems, dementia or patients recovering from stroke or heart attack [2]. Since the sensor nodes are small and non-wired, they provide a comfortable monitoring tool for patients, either when they are located in hospitals or at home. As an example, the WSN nodes detecting acoustic

vibration are used in falling detection of patients, where the data is connected to the internet or to the Global Positioning System (GPS) in order to provide help and rescue the patients [5].

- **Environment and agriculture:** weather forecast is a common environmental application for WSN, in which the sensor nodes report the ambient temperature, humidity, amount of rain, wind speed and direction. Precision agriculture is an example of WSN used in agriculture. Traditional farming treats large fields uniformly, in terms of the soil type and nutrient content, leading to inefficient use of farming resources. Precision agriculture is a farming method that depends on the data provided by the WSN to optimize the farming resources, and hence increase the farm yield [2].

- **Transportation and traffic:** while building and expanding roads is not always possible to solve the problem of traffic congestions, WSNs are used to monitor and manage the traffic providing less expensive and effective solution. As an example, the WSN nodes equipped with camera or radars are able to count the number of cars passing through a specific road, where they are capable to change dynamically the road speed limits, and prevent traffic congestion [2].

- **Industry:** detecting oil, water or gas leakage is a common WSN industrial application. The pipelines management is a challenging task, because of their long length, weight and harsh environment location. The WSN provides an effective method to monitor and report pipeline leakages [2].

1.2 Power Reduction in WSN

Figure 1.2 shows a star topology of a WSN consisting of a single base station and multiple sensor nodes, as well as the basic structure of the nodes. During the communication process, some of the sensor nodes are active, while others are not. Therefore, power reduction techniques are needed to improve the energy efficiency of nodes and increase their operation lifetime. In this section, a brief overview of the most common techniques used in WSN power reduction are presented.

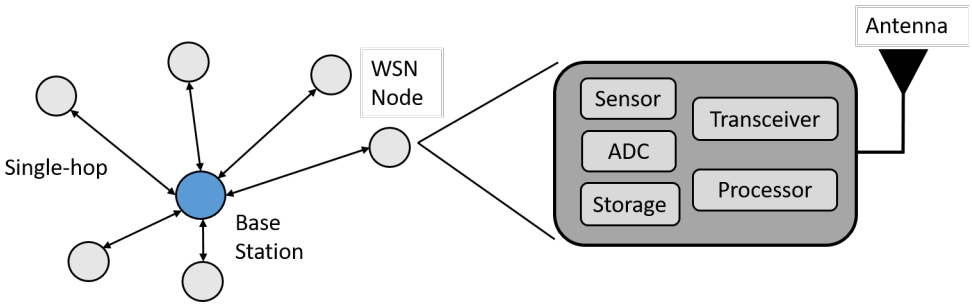


Figure 1.2: *A star topology WSN and the WSN node structure*

Energy Harvesting

The WSN nodes powered-up using an energy harvesting technique have unlimited operating lifetime. Several energy sources are used in the energy harvesting such as RF energy harvesting, solar power or vibrations in the WSN node's environment [6]. The extracted energy is converted and used to charge or even replace the batteries in the WSN nodes. There are several limitations in the energy harvesting techniques, for example RF energy harvesting suffers from high power loss between the RF signal source and the receiver, which makes the energy harvesting efficiency dependent on parameters such as the average transmitted power, the frequency and the communication distance. Figure 1.3 shows the basic block diagram of an RF energy harvester.

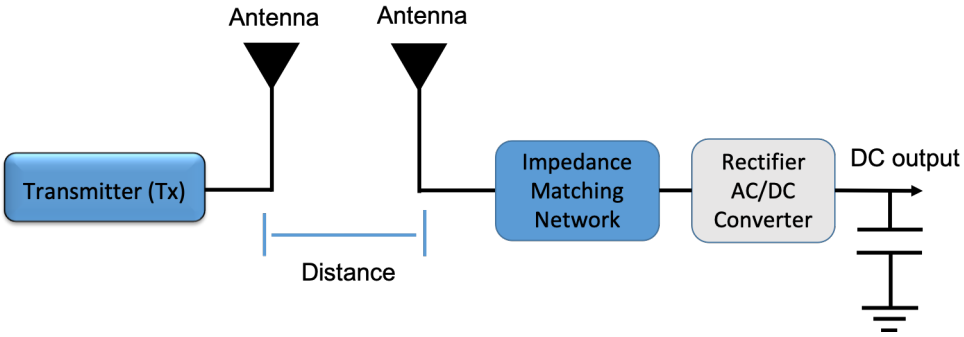


Figure 1.3: *RF energy harvester block diagram*

The RF energy harvester is composed of an antenna, followed by an impedance matching network to increase the power delivery to the AC/DC converter, which converts the RF signal into DC voltage. Several approaches of AC/DC can be used, such as voltage multiplier circuit. The rectified voltage is stored in a storing element such as capacitors [6], [7].

Duty Cycling

Depending on the WSN application scope, the network response time differs. Real-time applications such as industrial machine monitoring require fast information exchange, while other applications like weather forecast tolerate longer response time. The duty-cycling energy reduction method reduces the idle node listing time, and hence decreases the amount of power dissipation. Duty-cycling technique trades-off the network reliability and performance with the energy saving and sensor lifetime extension. Figure 1.4 shows the duty-cycling communication protocol. Since the transceiver is considered the most power dissipating component, the duty-cycled communication protocol activates the transceiver for a specific time-slot, in which it communicates with the base station and exchanges information, otherwise the nodes stay in low-power sleep mode resulting in a power dissipation reduction, but with an increase in data-latency and reduced network reliability [2], [3].

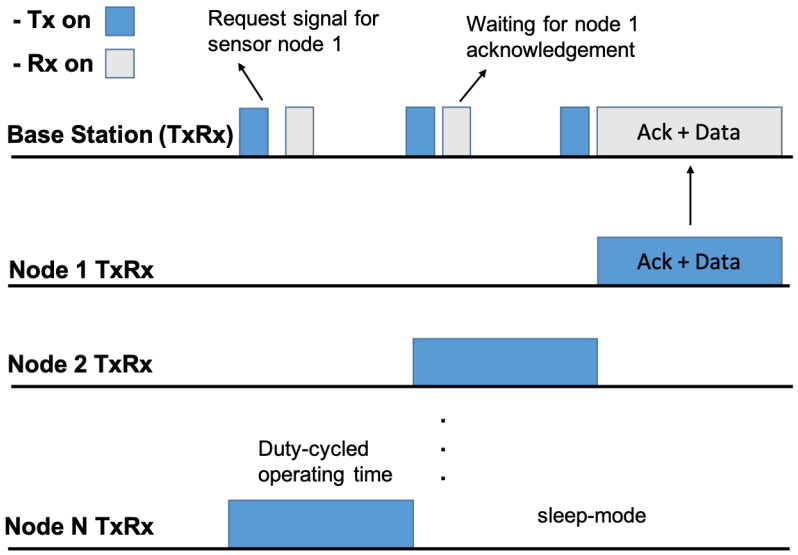


Figure 1.4: *Duty-cycling-based WSN communication protocol*

Wake-up Receiver

The WuRx is a low-power receiver that is integrated in each WSN sensor node as shown in Figure 1.5. The WuRx provides an asynchronous and on-demand communication scheme with the base station or between WSN nodes. The asynchronous communication scheme reduces the active-time of the WSN nodes, and hence decreases its power dissipation levels.

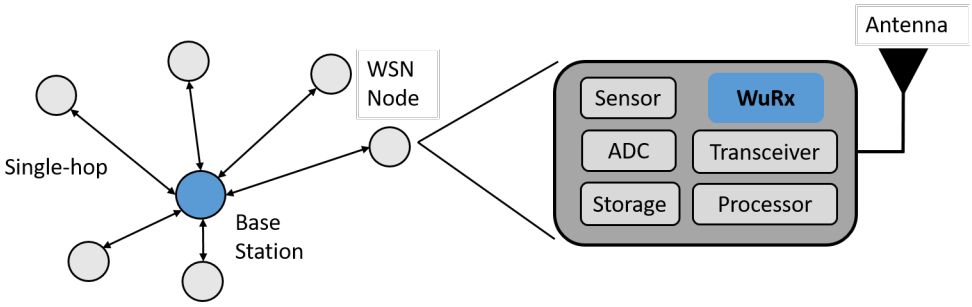


Figure 1.5: *WSN node with an integrated WuRx*

As shown in Figure 1.6, the role of the WuRx is to assert a wake-up signal to the required sensor node, so the communication starts with the base station or with other WSN nodes. In case the required sensor node ID matches the transmitted sensor node ID sent by the base station, a wake-up signal is asserted. Once the communication process is finished, the sensor node goes into sleep-mode. The WuRx is designed to be always-on, so that it can receive signals from the base station at any time. The WuRx exhibits low-power dissipation due to a radio architecture that is optimized specifically for always-on operation, low data-rate, simple protocol and appropriate modulation scheme to achieve low-power dissipation. From Figure 1.6, node 1 is only active for a short time, while other nodes stay in sleep-mode. All the nodes have an always-on WuRx, which dissipates a constant low level of power.

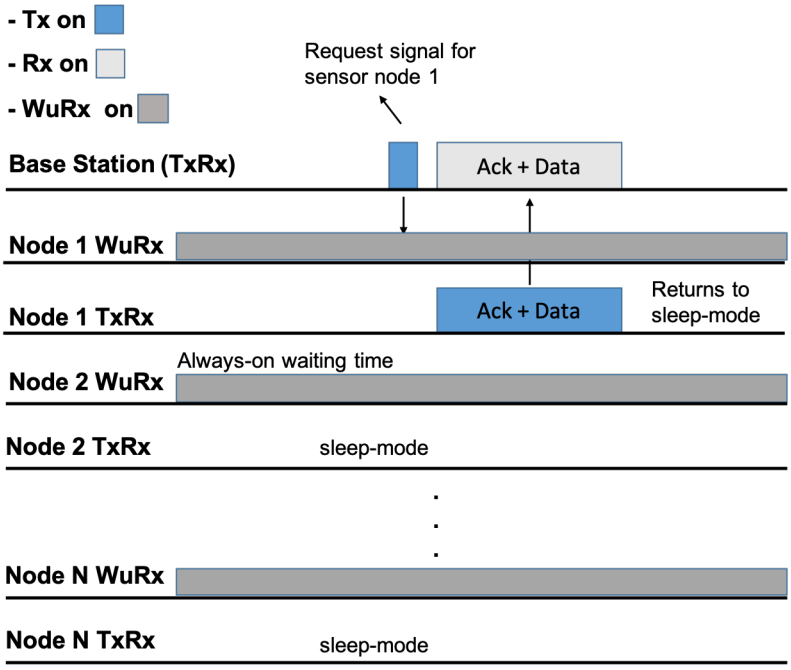


Figure 1.6: *Integrated WuRx-based WSN communication protocol*

Comparing the three power reduction techniques, the RF energy harvesting technique suffers from low-received signal power due to the free path power losses between the transmitter and the receiver, and hence works for short wireless communication distances. On the other hand, harvesting ambient light is a good option, but availability of the light is not always guaranteed. The duty-cycling communication protocol provides an efficient power dissipation method, but trades-off the network reliability and response time with the power dissipation level, which is unacceptable for wide range of WSN applications. The WSN with an integrated WuRx, which is the scope of this thesis, provides an asynchronous, real-time, and on-demand communication, and hence reduces the level of power dissipation, which makes it an appropriate design approach for a wide range of WSN applications.

1.3 Main Contributions

The thesis focuses on low-power WuRx as the most critical component of the system. The thesis main contributions are the following:

- Introducing the use of Surface Acoustic Wave (SAW) correlator as a passive RF signal detection stage to improve co-channel interference robustness and increase the Signal-to-Noise Ratio (SNR) in low-power receivers. Two different modulation schemes of correlators are discussed, the Linear Modulation Frequency (LFM), and the Barker-coded based SAW correlator. Based on a feasibility study carried out in [8], [9], a 2.44 GHz 13-bits Binary Phase-shift Keying (BPSK) Barker-coded SAW correlator is designed and fabricated on Lithium Niobate $LiNbO_3$ Piezoelectric substrate. The device is measured and characterized in frequency and time-domain. The measured SAW correlator has Insertion Losses (IL) of 12 dB, while

providing an amplitude compression gain of 5 dB, making the amplitude gain equals to Av = 0.42, when 13-bits Barker-coded signal is used as an RF excitation input signal, while other in-band signals are subject to 12 dB of power loss. The design, fabrication and measurements of the device were published in [A1].

- Verification of co-channel interference robustness provided by the 13-bits BPSK Barker-coded SAW correlator using discrete devices mounted on an RF PCB. The PCB is tested with three different RF excitation inputs at 2.44 GHz, such as 13-bits BPSK Barker-coded signal, WiFi and sine wave. The detected and amplified output signal as a result of the 13-bits Barker-coded excitation signal is 5 dB to 6 dB larger, when compared with the detected/amplified WiFi or sine wave signal at 2.44 GHz. The measurements were published in [A2].
- Design, fabrication and measurements of a WuRx Integrated Circuit (IC) in CMOS TSMC65n technology. To achieve low-power dissipation levels, direct-detection receiver architecture is selected in combination with 13-bits BPSK Barker-coded SAW correlator. The design introduces an innovative communication scheme, which depends on 13-bits BPSK Barker code along with Pulse Position Modulation (PPM). Furthermore, in order to improve the receiver sensitivity, the baseband bandwidth is reduced by means of an innovative Narrowband Correlator (NBC), which allows for scalable receiver sensitivity versus data-rate. The receiver achieves a power dissipation of 142 μW from 1.2 V supply source and sensitivity of −44 dBm and −50 dBm at a data-rate of 2 Mbps and 600 kbps respectively. The WuRx system and sensitivity analysis were published in [A3]–[A5], while the chip design and measurements were published in [A6], [A7].

1.4 Thesis Organization

The target of this thesis is to realize a low-power WuRx to be integrated into WSN nodes, so that the node power dissipation is reduced and the WSN operating reliably and lifetime are increased. The WuRx has to be always-on, and should exhibit a good robustness against co-channel interference.

Chapter 2, is an overview of common proposed design and architectures of RF radios, addressing their working principles and main design parameters, with emphasis on recent approaches of low-power WuRx design. Three main WuRx working schemes are discussed, the always-on, the duty-cycled and the multi-stage WuRx, with focus on the always-on WuRx architecture. The architecture of each proposed WuRx is discussed, in addition to its performance parameters. Subsequently, common circuit-level power reduction techniques and technologies that are commonly used in low-power RF radios are discussed in detail. A passive techniques to provide co-channel interference robustness in direct-detection receivers is also discussed. The chapter also demonstrates the proposed WuRx architecture, explaining the architecture block diagram and design requirements.

In chapter 3, top-to-bottom system-level analysis is presented. The WSN design considerations are discussed, explaining their basic sensor nodes architecture and basic communication scheme. Subsequently, the SAW correlator working principle is explained. Two main SAW correlator design schemes are analyzed. The LFM and the Barker-coded SAW correlators, addressing their performance parameters, fabrication feasibility and device

size. The chapter explains in details the analytical analysis of the WuRx communication sensitivity and communication range. The chapter ends with definition of the WuRx chip design targets.

The WuRx components design and simulation of both off-chip and the receiver IC implemented in CMOS TSMC65n technology are detailed in Chapter 4.

Chapter 5 reports the receiver measurements and results, as well as the measurements environment and setup, while chapter 6 states the thesis conclusion and outlook.

2 Related Work

This chapter presents an overview of conventional RF receivers, addressing their architecture and design parameters. In addition, several commonly known low-power WuRx architectures are discussed. The discussion is divided into three main working schemes. The always-on, the duty-cycled and the multi-stage WuRxs, with the emphasis on always-on working scheme. The chapter also presents circuit techniques that are mainly used in the design of low-power receivers. In addition, an overview of passive methods for the improvement of co-channel interferer robustness are given. In this chapter, the WuRx design requirements are defined, including power dissipation and communication performance. Depending on the WuRx architecture exploration given in this chapter, an SAW correlator based direct-detection WuRx architecture is proposed, which provides a low-power dissipation approach compared to the coherent receiver architecture. The proposed architecture is composed of off-and on-chip parts. The on-chip part implements the direct-detection low-power receiver designed and fabricated in CMOS TSMC65nm technology, while the off-chip part consists of an SAW correlator that provides a passive increase in the SNR of the WuRx IC RF input signal, and achieves robustness against co-channel interferers.

2.1 Conventional RF Receivers

The choice of RF receiver architecture significantly affects its performance parameters, such as receiver sensitivity, communication range, data-rate and robustness against noise and interferers. Beside differences in the working characteristics, the radio architectures have different levels of design complexity, size, power dissipation and cost. The choice of a receiver architecture depends on the system requirements and the scope of the application. This section discusses several proposed RF radios based on conventional receiver architectures such as coherent, non-coherent and backscattering architectures, addressing their basic building blocks, working principle and their main characteristics.

2.1.1 Coherent Detection

In coherent detection RF radios, the input RF signal is multiplied with a Local Oscillator (LO) signal, thus generating an Intermediate Frequency (IF) signal. The IF signal is then filtered, demodulated and amplified. Figure 2.1 shows the basic building blocks of heterodyne RF receiver [10]. The input RF signal is filtered by a Band Pass Filter (BPF) that selects the desired receiver bandwidth and rejects out-of-band signals. The filter is followed by a Low Noise Amplifier (LNA), which is an RF amplifier that amplifies the input RF signal with low Noise Figure (NF). The LNA is followed by an Image Rejection (IM) filter, that filters-out the LO image frequency. The signal down-conversion is done in the RF mixer, where the input RF signal is multiplied with sinusoidal ω_{LO} signal generated by the LO, where the generated signal has components at $\pm(\omega_{RF} \pm \omega_{LO})$.

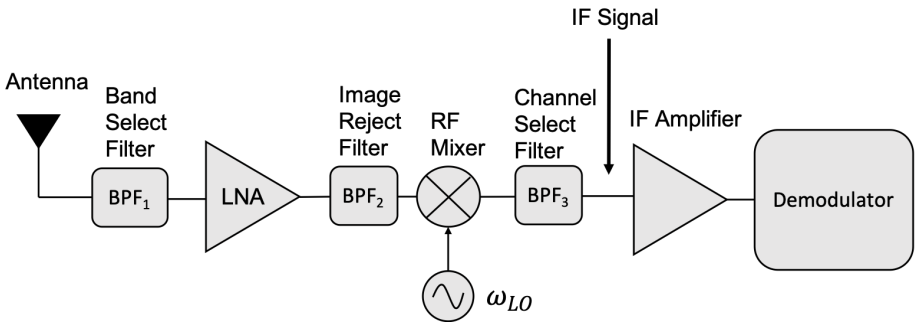


Figure 2.1: *Basic block diagram of heterodyne RF receiver [10]*

The Channel Select Filter (CSF) filters-out the undesired down-converted components, and keeps only the IF components, which is equal to $\omega_{IF} = \omega_{RF} - \omega_{LO}$. The IF signal is amplified by an IF amplifier in order to have sufficient amplitude for demodulation [11]. The heterodyne RF receiver exhibits a complex receiver design with multiple off-chip components, which increases the design size and cost. The IR filter (BPF_2) in Figure 2.1 is bulky and highly selective filter, which makes it difficult in a monolithic system integration. In addition, it acts as a $50\,\Omega$ load to the LNA, adding more complexity to the LNA design and preventing the LNA to be integrated with subsequent circuits such as the RF mixer and the LO. On the other hand, the heterodyne receiver has highly linear LNA, RF mixers and LO, which achieves high receiver sensitivity and co-channel interference robustness, however it results in a significant increase in the level of power dissipation [10].

2.1.2 Non-Coherent Detection

The main difference between coherent and non-coherent RF radio architectures is the absence of the LO in the non-coherent detection that is used along with the RF mixer circuit to down-convert the received RF to IF signal. The non-coherent receiver down-converts the RF signal using a squaring-law circuit such as an RF envelope detector. Figure 2.2 shows the basic block diagram of a non-coherent RF receiver [10], [12].

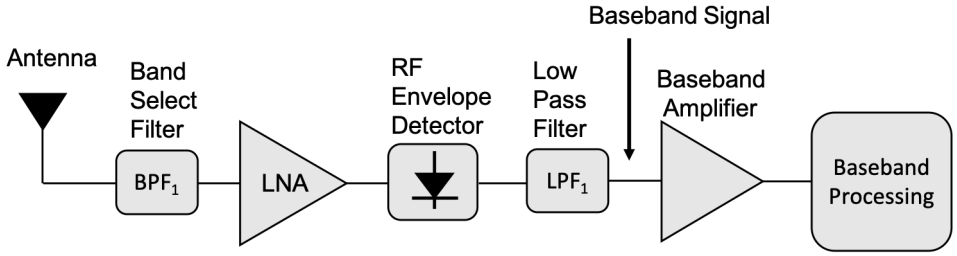


Figure 2.2: *Basic block diagram of a non-coherent RF receiver [12]*

The input RF signal is filtered by a BPF that selects the desired receiver bandwidth and rejects out-of-band signals, and then amplified by a LNA. The amplified input RF signal is detected and down-converted by an RF envelope detector, which is based on Schottky

diodes, or for a better performance and higher sensitivity, an active RF envelope detection is used. The high frequency signal components are filtered-out by a Low Pass Filter (LPF) and then the baseband signal is amplified by the baseband amplifier before entering the baseband processing circuit [12]. The non-coherent receiver architecture exhibits less design complexity compared to the coherent receiver, and it is realized as a monolithic system, which reduces cost and size. In addition, the proposed receiver fulfills the emerging demand of low-power and low data-rate receivers. However, the non-coherent receivers suffer from high noise bandwidth, and hence reduced receiver sensitivity and data-rate, as well as poor performance against co-channel interferers [A2].

2.1.3 Backscattering Radios

Backscattering Radio Frequency IDentification (RFID) is a known application that uses the backscattering radio architecture. An RFID is used in short range wireless applications such as Electronics Product Code (EPC) reading, in which the product has a fixed tag that uses backscattering modulation to communicate the information with the nearby RFID reader [13], [14]. Figure 2.3 shows the basic block diagram of RFID communication system [13]. The RFID reader sends continuously the RF signal and observes the backscattered modulated RF signal. The tag input impedance is intentionally mismatched so that the excitation signal is scattered back to the reader. The RFID tag uses this working principle to encode the information that is interpreted on the RFID reader side. The RFID tag is a passive radio that is powered-up by the RF energy harvested from the reader Continuous Wave (CW) signal.

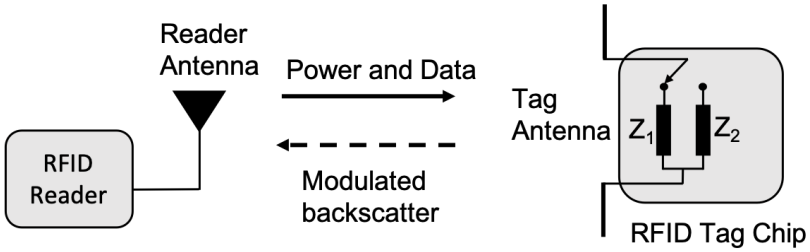


Figure 2.3: *Basic block diagram of an RFID tag with two modulator states [13]*

On the RFID tag side, alternating between the antenna impedance load values Z_1 and Z_2 achieves a binary modulated scattered signal. The backscattering RFID is a passive receiver that allows for no-power receiver design, however, it depends on the RF energy harvesting for powering-up the circuit, which works for short distances, and it is inappropriate for WSN that is geographically distributed over large physical area. In addition, a near high-power co-channel signal source makes the proposed RFID receiver blind [13].

2.2 Wake-up Receivers Architectures

In this section, a design overview of several proposed WuRxs is presented. For each receiver, the basic architecture, working principle and characteristics are pointed out. The

section is split into three main WuRx working schemes: always-on, duty-cycling and multi-stage, with emphasis on the always-on approach, which is the scope of this dissertation.

2.2.1 Always-on

Always-on WuRx listens continuously for wake-up calls transmitted by the base station or other WSN nodes. The use of the asynchronous communication scheme in always-on WuRx reduces the issue of network latency, but adds design challenges on the power dissipation level, since the receiver must be always listening. The WuRx proposed by [15] uses super-heterodyne receiver architecture along with the principle of uncertain-IF down-conversion. The receiver works at 2 GHz with On-Off Keying (OOK) signal modulation scheme and is designed and fabricated using CMOS 90 nm technology. The signal spectrum for the uncertain-IF working principle is shown in Figure 2.4. The signal is filtered-out by a CSF to remove interferers and out-of-band signals. The filtered signal is mixed with the LO, where its frequency is not well-defined and the LO frequency variation is lying between $\pm BW_{if}$ of the IF bandwidth that equals to 100 MHz.

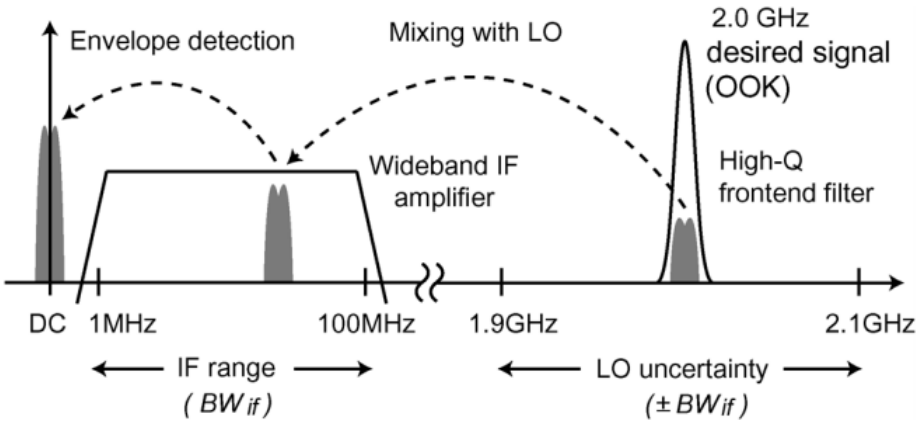


Figure 2.4: *Uncertain-IF receiver signal spectrum [15]*

The not well-defined LO allows for less complex oscillator design and reduction in the LO power dissipation. The IF signal is then amplified by an IF amplifier, which is more power-efficient compared with an RF signal amplifiers such as LNA. The amplified signal is detected by means of an envelope detector, where it is converted from IF to DC spectrum. The block diagram of the uncertain-IF receivers is shown in Figure 2.5. The input RF OOK signal is filtered by a narrowband impedance matched filter that contains a high Q-factor Bulk Acoustic Wave (BAW) filter. The input matching network provides a passive voltage boost of 12 dB at the input of the signal mixer. The RF mixer circuit converts the input RF signal to uncertain-IF signal. The mixer uses the free-run LO that is digitally controlled to center its frequency within the IF band despite the process and temperature variation that affects the oscillator. The down-converted signal is amplified using a wideband IF amplifier of 100 MHz bandwidth. The subsequent circuit is the envelope detector, which converts the uncertain-IF signal into DC. The proposed receiver achieves a sensitivity of -72 dBm, data-rate of 100 kbps and Bit Error Rate (BER) of 10^{-3}, while dissipating 52 μW from 0.5 V power supply. The proposed receiver uses super-heterodyne

architecture, which achieves a high receiver sensitivity. The principle of uncertain-IF frequency allows for low-power receiver design, specifically the free-run LO oscillator and the IF band amplifier. However, due to process variation and temperature changes, the LO center frequency is difficult to predict and control.

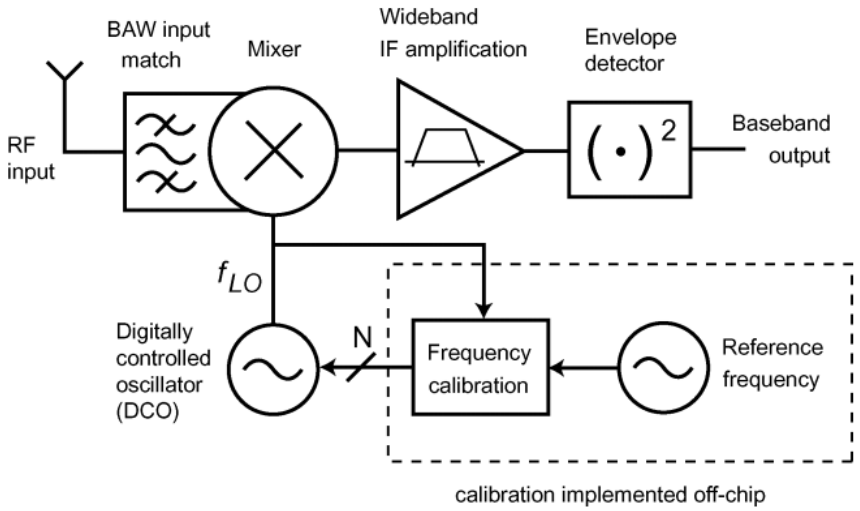


Figure 2.5: *Block diagram of uncertain-IF receiver architecture [15]*

Another always-on WuRx is proposed in [16], which uses direct-detection architecture. The receiver uses OOK input signal modulation at 2.4 GHz/ 915 MHz, and is implemented in CMOS 90 nm technology. The total power dissipation is 51 µW from 0.5 V voltage supply. The receiver sensitivity at 915 MHz is −75 dBm at a data-rate of 100 kbps, while at 2.4 GHz, it achieves a sensitivity of −64 dBm and −69 dBm at data-rate of 100 kbps and 10 kbps respectively. The design main contribution is to reduce the receiver noise so that the communication sensitivity is improved. The block diagram of the double-sampling receiver is shown in Figure 2.6.

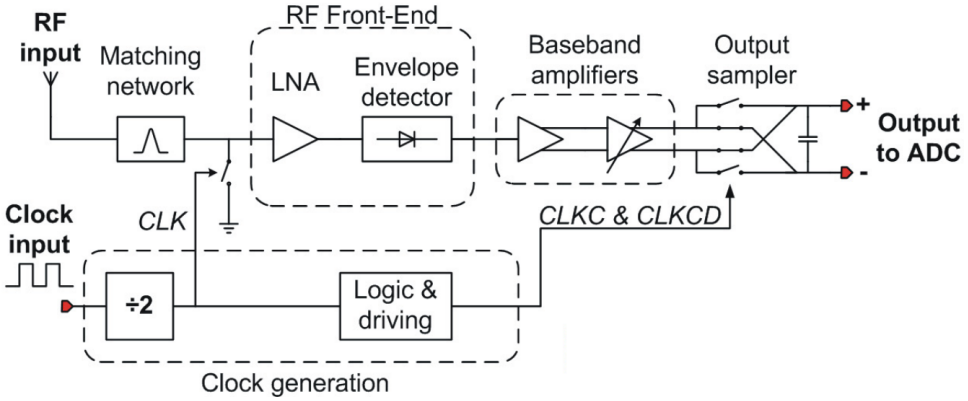


Figure 2.6: *Block diagram of double-sampling WuRx [16]*

The method of double-sampling is applied to the down-converting front-end to suppress the offset and the flicker $1/f$ noise. The receiver is designed to reduce the data-rate and to narrow down the output bandwidth resulting in an improvement in the total receiver sensitivity. The receiver impedance matching network is composed of an off-chip capacitive

transformer and high-Q off-chip inductor so that the receiver operates at different input frequencies. The RF LNA amplifies the input signal, which is alternating between ground and antenna input. The RF envelope detector converts the RF signal into baseband. As a subsequent stage, the baseband amplifier amplifies the baseband signal to an appropriate level before the double-sampling technique takes place, and converts the detected and amplified signal to DC. The doubled-sampling technique distinguishes the desired signal from noise, and improves the receiver SNR. As shown in the receiver signal propagating spectrum in Figure 2.7, the input RF signal is modulated by a switch at the input of the receiver front-end, and produces double-sided signal spectrum that is away by f_{CLK} from the carrier signal f_C on each side. The RF envelope detector converts the signal to baseband signal around f_{CLK} instead of DC. To reduce the noise-level, the double-sampling frequency f_{CLK} is chosen to be beyond flicker noise, which is 10 MHz in the proposed design, making the down-converted signal away from the flicker noise. The baseband signal is then amplified and converted to DC. The flicker $1/f$ noise and offset is filtered out, resulting in an improvement of the receiver sensitivity. The proposed double-sampling receiver in [16] uses an efficient method to reduce noise-level, on the cost of reducing communication data-rate, which has less priority in the WuRx design requirements when compared to power dissipation and sensitivity. However, the total power of 51 µW does not include the input clock generation of 20 MHz, which rises significantly in case it is included in the total receiver power dissipation budget. Additionally, the receiver is not robust against co-channel interferers.

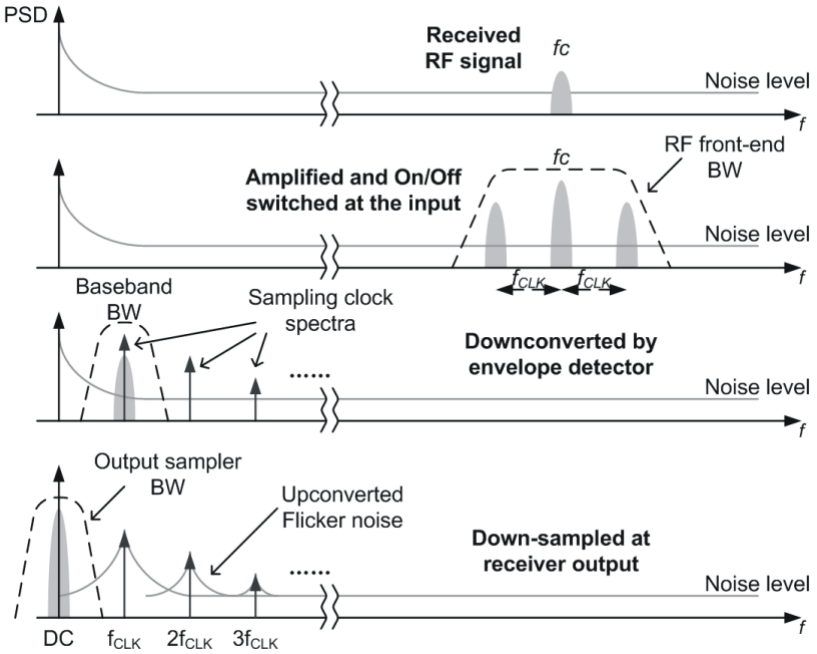


Figure 2.7: *Signal propagation spectrum [16]*

The WuRx proposed in [17] uses non-coherent and active direct-detection to detect and down-convert the RF signal to baseband. The proposed WuRx block diagram is shown in Figure 2.8. The receiver works at both 2.4/5.8 GHz frequencies with OOK signal modulation scheme, and is designed and fabricated using CMOS 180 nm technology. The use of an active RF detector allows for low-power front-end design instead of using LNA,

RF mixer and LO in coherent receiver architectures proposed in [10]. The subsequent circuit of the RF detector is a baseband Programmable Gain Amplifier (PGA) that adopts an open-loop design to allow for low-power design. The PGA gain ranges from 20 to 40 dB and achieves bandwidth of 4 MHz. The amplified baseband signal is demodulated and digitized by a 4 Mega Sample Per Second (MSPS) continuous-time first-order low-pass sigma-delta ΣΔ Analog-to-Digital Converter (ADC) with 16 Over Sampling Ratio (OSR).

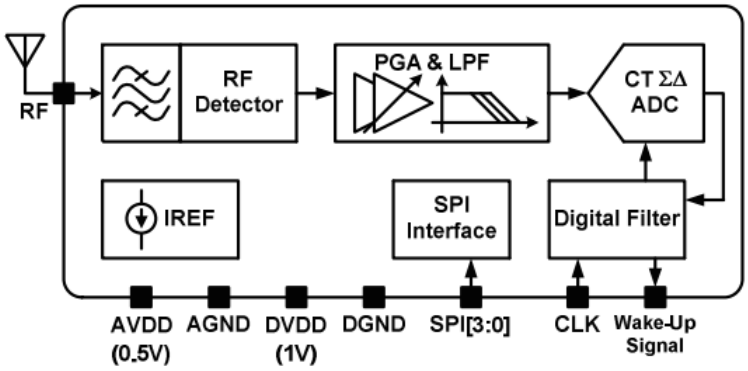


Figure 2.8: *Block diagram of the direct-active RF detection WuRx [17]*

The proposed receiver achieves a sensitivity of −65/−50 dBm at 2.4/5.8 GHz respectively. The receiver achieves a data-rate of 100 kbps at −65 dBm sensitivity, and dissipates a power of 10 µW. The proposed receiver in [17] dissipates five times less power than the receiver proposed in [15]. However the super-heterodyne architecture exhibits higher receiver sensitivity. In addition, the receiver is not robust against co-channel interferers.

A non-coherent Tuned RF WuRx is proposed in [18]. Its block diagram is shown in Figure 2.9. The receiver operates at 1.9 GHz and uses Tuned RF (TRF) receiver architecture to amplify, detect and down-convert the RF input signal to baseband.

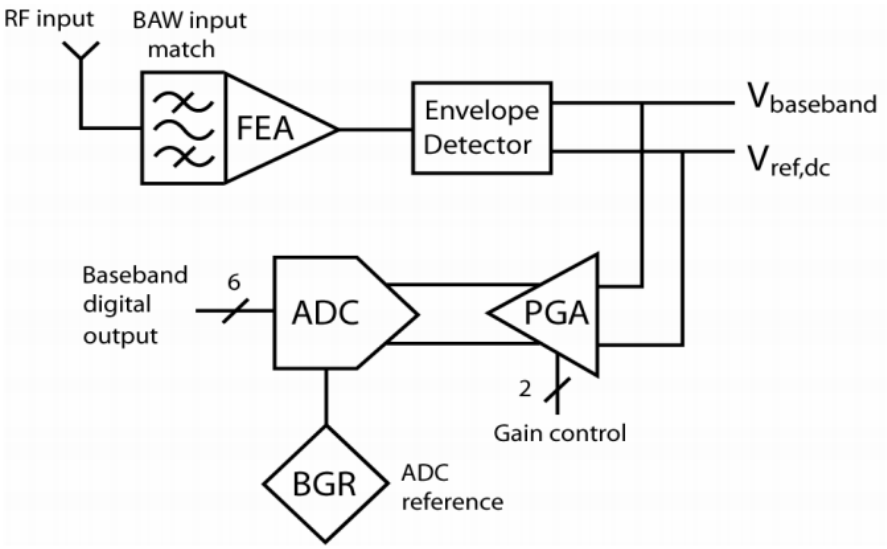


Figure 2.9: *Block diagram of the Tuned RF receiver architecture [18]*

The OOK modulation scheme is used to simplify the circuit complexity. The receiver is designed and fabricated in CMOS 90 nm technology and dissipates 65 µW from 0.5 V with a sensitivity of −48 dBm at a data-rate of 100 kbps. From Figure 2.9, the input OOK RF signal is amplified using the Front-End Amplifier (FEA) with a gain of 10 dB. The RF signal is down-converted to baseband using an active RF envelope detector that operates in sub-threshold region. The analog detected signal is amplified by a PGA, which is followed by 6 bits resolution ADC. The receiver front-end operates in MOS transistor sub-threshold region, allowing for low-power design. The use of the BAW provides a narrowband matching and filters out-of-band interferers. However, it does not provide a method against co-channel interferers.

Another ultra-low-power WuRx is proposed in [19]. The receiver block diagram is shown in Figure 2.10, where the receiver uses direct-detection architecture to down-convert the input RF signal to baseband. The design uses an external SAW filter and discrete components for impedance matching. The RF signal is detected by a non-linear envelope detector and is amplified afterwards. The detected signal suffers from low SNR, therefore the proposed receiver uses a low-power analog/mixed-signal correlator unit for digital 64-bit pattern with coding gain, in order to increase the receiver sensitivity. The wake-up threshold is configurable, such that a wake-up interrupt is asserted once the correlation result exceeds a specific wake-up threshold. Because there is no synchronization between the transmitter and the receiver, 128 parallel correlation stages are used. The receiver operates at 868 MHz and achieves a sensitivity of −71 dBm with a total power dissipation of 2.4 µW from 1 V power supply.

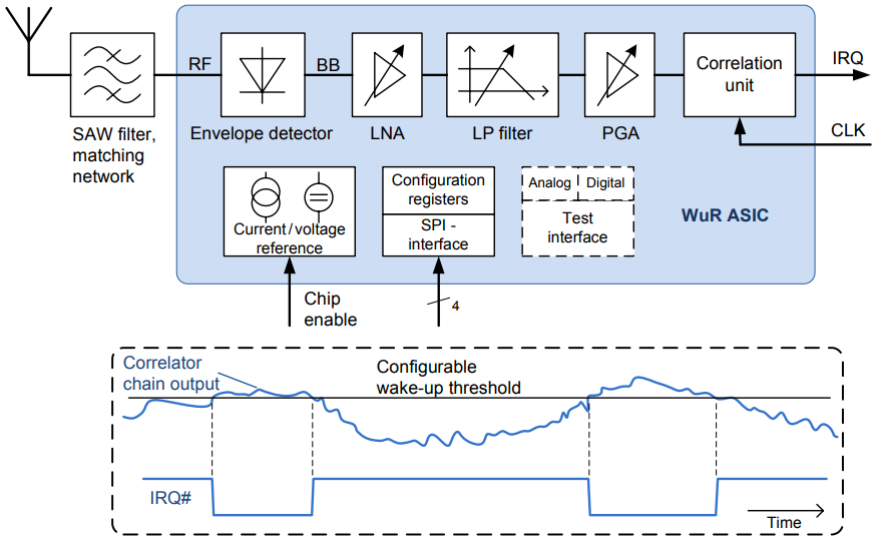


Figure 2.10: *Block diagram of WuRx ASIC (top figure). Working principle of the correlation unit (bottom figure) [19]*

The receiver proposed in [19] dissipates an ultra-low-power with a corresponding high sensitivity of −71 dBm. However the wake-up time, which is coupled with the correlation time of the baseband correlator is 7 ms, which is considered a long time for a wide range of real-time applications of WSN. Also to eliminate communication synchronization, complex 128 parallel circuits are added, which increase the receiver size and design

complexity. In addition, co-channel interference robustness is not considered in this approach.

2.2.2 Duty-cycling

The proposed receiver in [20] scales power dissipation levels versus communication data-rate at specific receiver sensitivity. Periodic receiver switching on-and-off is used to reduce the power dissipation of the receiver. The average receiver current dissipation is expressed in Equation (2.1).

$$\bar{I}_{RX} = \frac{T_{on}}{T_{on} + T_{off}} . I_{RX,on} \tag{2.1}$$

Where the switching duty-cycle is defined by the ratio between T_{on} and $T_{on} + T_{off}$. Equation (2.2) defines the sampling frequency f_A, which is greater than the duty-cycle switch-on time. The receiver settling time $t_{s,i}$ define the minimum duty-cycle time, and hence the lowest power dissipation operating point.

$$\frac{1}{f_A} = T_A >> T_{on} > t_{s,i} \tag{2.2}$$

According to the duty-cycled proposed receiver in [20], a case of 31-bits data packet is demonstrated. As it is shown in Figure 2.11, the bit-time is defined as T_b and equals to 1 ms, which makes the packet-time 31 ms. At a 100 ns of receiver settling time, the receiver dissipates 11 mA in always-on operating case. Selecting duty-cycle of 0.1 % dissipates 11 µA at a data-rate of 1 kbps.

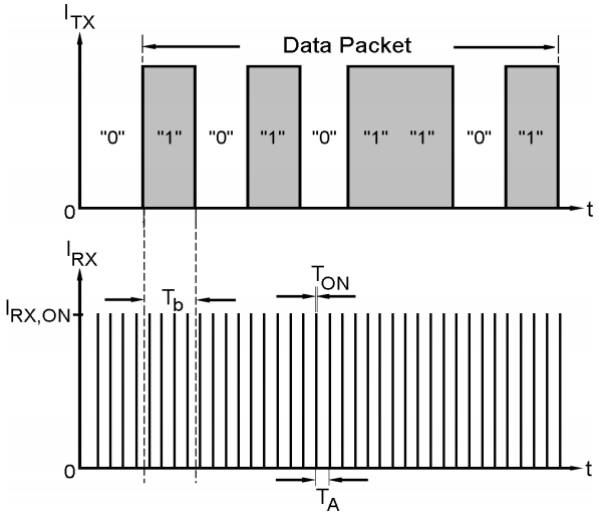


Figure 2.11: *Asynchronous over-sampling of OOK modulated data bits [20]*

From Figure 2.11, the receiver switched on-and-off in pulse operation with asynchronous over-sampling, the sampling period T_A equals an integer of the bit length T_b. In the proposed design, the sampling period equals four-times the bit length. The average current dissipation is expressed in Equation (2.3).

$$\bar{I}_{RX} = \frac{4T_{on}}{T_b}.I_{RX,on} = T_{on}f_A I_{RX,on} \tag{2.3}$$

The receiver block diagram is shown in Figure 2.12. The proposed receiver uses the super-heterodyne receiver architecture. The receiver operates at 868 MHz and uses OOK modulation scheme. It is designed and fabricated using CMOS IHP 130 nm technology and achieves a sensitivity of −83 dBm. From Figure 2.12, the receiver is composed of BSF followed by an LNA with a gain of 18 dB and designed to have fast settling time. The RF signal is down-converted by means of a fully differential Gilbert cell with a conversion gain of 10 dB to an IF-frequency of 33 MHz. The IF signal is converted to DC using an envelope detector and the pulse controller defines the duty-cycle. The proposed receiver uses the over-sampling technique to overcome the absence of synchronization between the receiver and the transmitter. The receiver achieves a high sensitivity due to the use of the super-heterodyne receiver architecture. In addition, an ultra-low-power dissipation is achieved, but at low data-rate of 1 kbps and receiver response time of 31 ms. Improving the receiver response time by scaling the data-rate increases the current dissipation dramatically to reach 1.1 mA at a data-rate of 100 kbps.

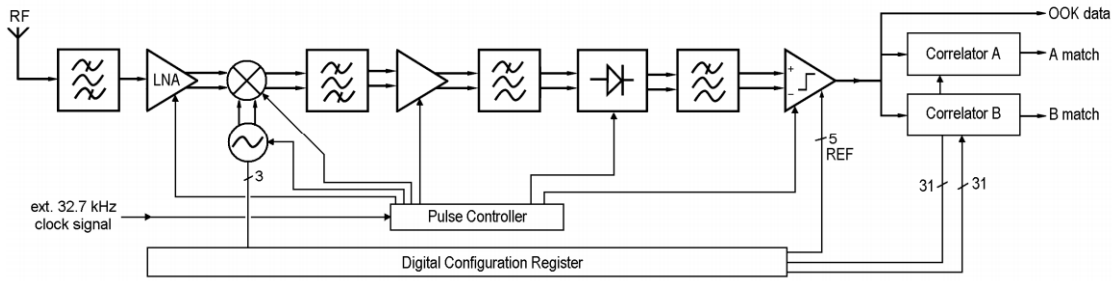


Figure 2.12: *Block diagram of the proposed duty-cycle based WuRx [20]*

2.2.3 Multi-stage

The wake-up scheme based on multiple-stage inserts an intermediate stage into the receiver design, which is conditionally activated by the receiver's first power detector stage. A three-stage WuRx is proposed in [21], [22], where the WuRx block diagram is shown in Figure 2.13. The first stage in the proposed receiver is an always-on stage that dissipates a nano Watt order of magnitude O(nW) power and exhibits less design complexity if compared with the second stage that dissipates micro Watt order of magnitude O(μW). The second stage is only activated if a certain power level is detected by the first stage. An LNA is added in front of the detector in the second stage to increase the receiver sensitivity. The transmitted address signal is decoded in the address decoder, and if it matches the receiver internal address, a wake-up signal is asserted to activate the main nodes transceiver. The wake-up sequence is shown in Figure 2.14. Adding the intermediate stage reduces the amount of false positive wake-up signals to the main node transceiver. However the number of false wake-up signals to the second stage is not addressed, considering that the LNA dissipates considerable amount of power.

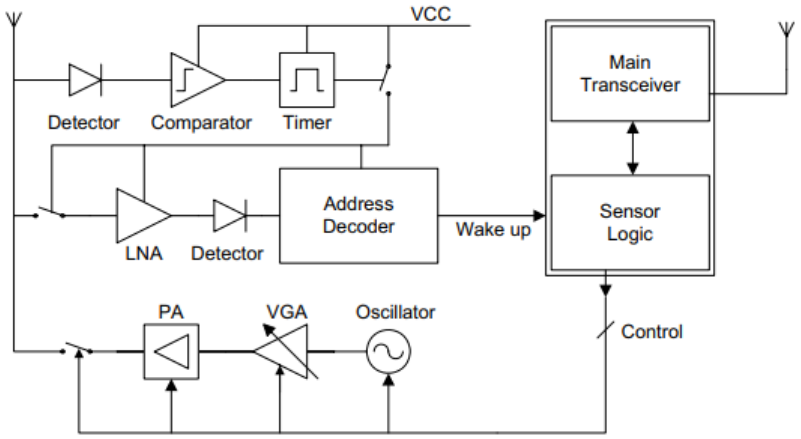


Figure 2.13: *Three stages WuRx block diagram [21]*

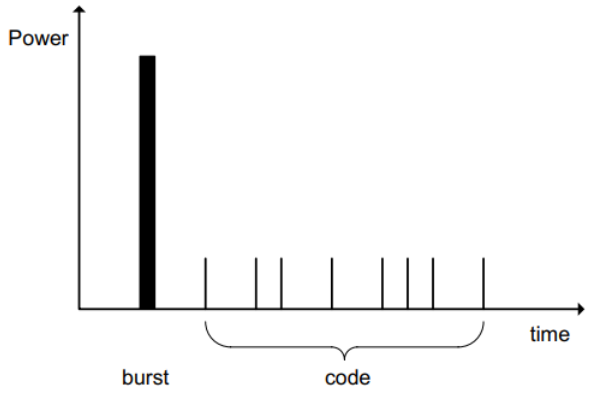


Figure 2.14: *Wake-up sequence [21]*

2.3 Circuit Techniques

Power dissipation in circuits has multiple sources. The first is the static power dissipation, which is due to the circuit DC biasing. Dynamic power dissipation is the second major power dissipation source, which results from the dynamic circuit switching. Leakage and short circuit currents are another power dissipation sources, where the total power dissipation is defined by summing-up the four quantities [23]. Section 2.2 discussed several WuRx proposed architectures to achieve low-power designs. However, the circuit-level design techniques play a significant role in reducing the power dissipation on the circuit level without trading-off the design objective. Several common circuit design methods that are used in low-power receivers are discussed in this section.

2.3.1 Sub-threshold Region

CMOS circuits working in weak-inversion region, which is also called sub-threshold region, dissipates power in micro Watt levels, making it a suitable operating region for low-power applications. The transistor current in weak-inversion region decreases expo-

nentially, when the gate-to-source voltage is below the transistor threshold voltage. The threshold voltage point is defined by the transistor strong inversion characteristics [24], [25]. Considering N-channel MOSFET operating in strong-inversion region, the voltage applied on the gate is large enough to push the holes from the channel surface, leaving behind the electrons attracted to the surface, creating a strongly inverted channel. While in weak-inversion operating region, the mobile charges Q_i in inversion region are much smaller than the depletion charges Q_D, however, the charges of the electrons Q_i are still capable of carrying small current. The MOS current square-law used in strong-inversion is inaccurate to model the current behavior in sub-threshold region. The drain current in weak-inversion region has identical characteristics of a bipolar transistor with infinite current. The MOS transistor weak-inversion current is expressed in Equation (2.4).

$$I_D = I_{SPEC} e^{\frac{V_G - V_{TH}}{nV_T}} (e^{\frac{-V_S}{V_T}} - e^{\frac{-V_D}{V_T}}) \tag{2.4}$$

Where the process parameter $I_{SPEC} = 2n\beta V_T^2$. V_{TH} is the transistor threshold voltage, V_T is the thermodynamic voltage, which equals $\frac{kT}{q}$. k is Boltzmann constant, T is the ambient temperature, q is the electric charge and n is sub-threshold swing coefficient. $\beta = \mu C_{ox} \frac{W}{L}$, where μ is the mobility of the carriers in the channel, C_{ox} is the gate-oxide capacitance per unit area, and W/L is the effective transistor width over length ratio. Equation (2.4) is split into forward I_F and reverse I_R current components as expressed in Equation (2.5):

$$I_D = I_{SPEC} [I_F(V_G, V_S) - I_R(V_G, V_D)] \tag{2.5}$$

The channel current is expressed as the difference between the forward current, which is a function of the gate and source voltage and does not depend on the drain voltage, while the reversed current is a function of the gate and drain voltage and does not depend on the source voltage. Considering a common source biased transistor, where $V_S = V_B$, Equation (2.4) is further simplified as expressed in (2.6), giving that the condition of weak-inversion biasing is when $V_{GS} < V_{TH}$.

$$I_D = I_{SPEC} e^{\frac{V_G - V_{TH}}{nV_T}} (1 - e^{\frac{-V_{DS}}{V_T}}) \tag{2.6}$$

The weak-inversion region provides the maximum possible transconductance g_m, which is expressed in Equation (2.7). Due to the high value of g_m, the input transistor biased in sub-threshold region has reduced input-referred noise with respect to the saturation region biased transistors.

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} = \frac{I_{ds}}{nV_T} \tag{2.7}$$

In addition, weak-inversion transistors have lower saturation voltage $\leqslant 3V_T$, which allows for larger voltage swing at a low-power supply source. However, sub-threshold region circuits have reduced frequency response, which limits their applications in RF analog design. Increased leakage current is an additional drawback in sub-threshold circuits, which increases the power dissipation. In addition, due to the exponential characteristics of the current/voltages, the device mismatch and temperature variation have an increased effect on the circuit performance [23]. Refer to [23]–[26] for more details about sub-threshold region modeling and characteristics.

2.3.2 Power Supply Scaling

The level of power dissipation in circuits is directly related to the supply voltage. Reducing the supply voltage is a straight forward technique to reduce power dissipation in circuits, however it trades-off power with circuit performance. Scaling-down the transistor threshold voltage limits the performance, but also increases the static power dissipation [23], [27]. Another approach based on multi-supply voltage sources is used to reduce power dissipation in circuits. In this technique, two different levels of supply voltages are utilized. The higher voltage level is used in the critical circuit parts, which requires high performance and reduced noise levels (i.e RF front-end), and the lower voltage level is used in less critical circuit parts [28]. According to [23], scaling-down the supply voltage in analog circuit design is coupled with several design parameters, such as the channel threshold voltage. While changing the transistor channel length reduces its threshold voltage, further threshold voltage reduction is limited to specific noise floor, where the SNR is properly maintained. Assuming that NMOS transistor works in saturation region, the minimum used supply voltage is expressed below:

$$V_{DS} > V_{GS} - |V_{TH}| - V_{signal} \tag{2.8}$$

Equation (2.8) implies that even with the variation headroom of the threshold voltage, there is a minimum supply voltage level that can not be exceeded. The transistor speed is another parameter that is affected by the supply voltage scaling. The transistor f_{max} is dropped by the reduction of the supply voltage, therefore in RF analog design circuits, it is desired to maintain a high supply voltage. The input signal Dynamic Range (DR), which is defined by the ratio between the largest and the smallest signal amplitude is affected by the supply voltage variation. The input SNR is degraded with the reduction of the supply voltage, and hence the input signal dynamic range is reduced. Refer to [23] for more details.

2.3.3 Current Reuse

Low-power RF analog circuits benefit from the current-reuse circuit design principle to maintain circuit performance at low-current levels. According to [23], [29], the transistors transconductance is preserved with reduced current, which makes it a suitable approach for low-power applications. The power reduction in this case does not influence the design parameters related to transconductance such as linearity and gain. The current reuse working principle is illustrated in Figure 2.15. Figure 2.15(a) shows a single NMOS transistor with transconductance equals to g_m at (W/L) ratio, and the current equals to I_D. The objective of current-reuse design technique is to achieve the same transconductance g_{m1} and $\omega_T = g_{m1}/C_{gs}$ at a reduced current-level. In Figure 2.15(b), each NMOS transistor has $(1/2)(W/L)$ ratio and current value of $(1/2)I_D$, however the total transconductance $g_{m2,3}$ is equal to $g_{m2} + g_{m3} = g_{m1}$. Substituting the NMOS with PMOS transistor in Figure 2.15(c) makes the total transconductance equals to $g_{m4,5} = g_{m4} + g_{m5}$ at device ratio of $(1/2)(W/L)$ and current of $(1/2)I_D$.

This concept is used to design RF analog circuits such as LNA and RF mixers. The LNA proposed in [30] is a self-biased LNA, based on resistive feedback current-reuse circuit as

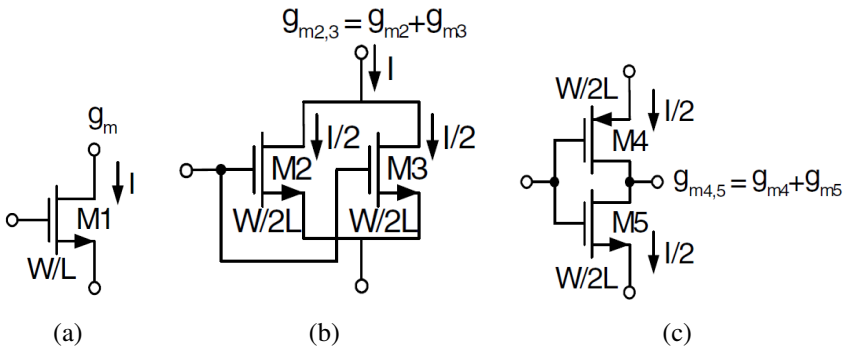


Figure 2.15: *Current-reuse working principle [29]*

shown in Figure 2.16. The circuit is implemented in CMOS 130 nm technology. The LNA dissipates 120 µW from 0.6 V voltage source, with 14.6 dB voltage gain and NF of 3.8 dB at 2.4 GHz. The supply voltage source is configurable with Digital-to-Analog Converter (DAC), so that the LNA works at lower voltage gain and power dissipation levels.

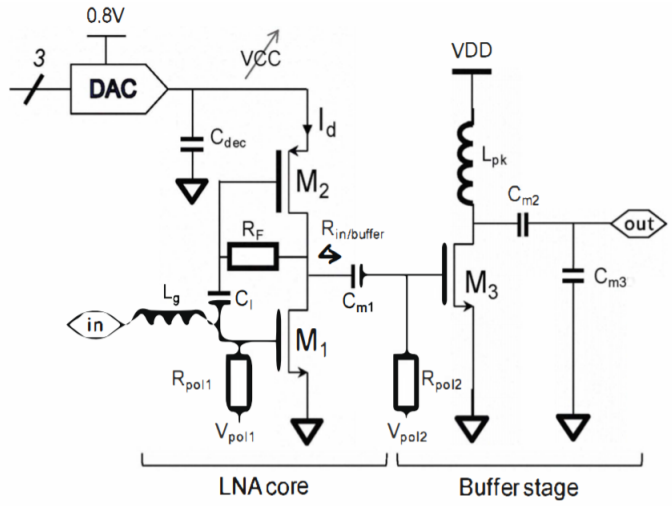


Figure 2.16: *Resistive feedback LNA schematic with buffer stage [30]*

The input stage is based on current reuse self-biased inverter amplifier. The LNA stage voltage gain is expressed in Equation (2.9).

$$A_v \simeq \frac{g_{mT}}{2R_s C_{gsT}\omega_0}.(r_{ds1} \parallel r_{ds2} \parallel R_F \parallel R_{in,buffer}) \tag{2.9}$$

Where according to the current-reuse working principle, $g_{mT} = g_{m1} + g_{m2}; C_{gsT} = C_{gs1} + C_{gs2}$. The real part of the LNA input impedance is a function of R_F, g_{mT}, C_{gsT} and $R_{in,buffer}$, while the imaginary part is cancelled by the gate inductor L_g. The current-reuse principle is also used in RF mixer design to provide low-power up or down RF signal conversion [31], [32]. The schematic of the proposed mixer in [32] is shown in Figure 2.17. The voltage to current conversion is doubled with the insertion of M_4, creating a current-reuse pair with M_1. The gate biasing of M_1 and M_4 is separated by an ac-coupled capacitor [31], [32]. The mixer voltage conversion is doubled as expressed in Equation (2.10).

In addition to the voltage gain improvement, the use of current-reuse principle in the voltage-to-current converter circuits increases the mixer linearity and NF [32], [33].

$$A_v = \frac{2}{\pi}(g_{m1} + g_{m4})R_L \tag{2.10}$$

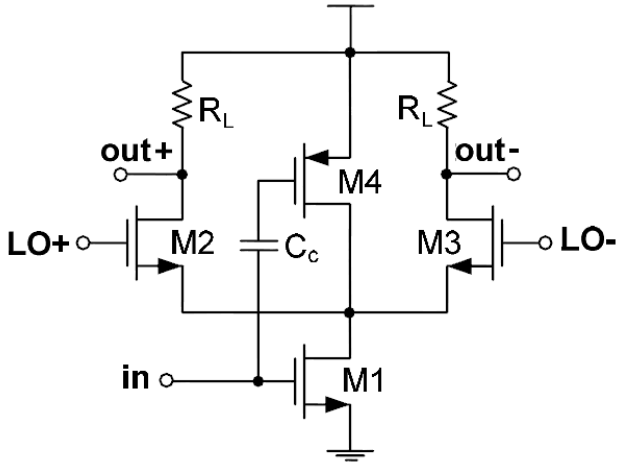


Figure 2.17: *Current-reuse based single-balanced Gilbert cell mixer [32]*

2.3.4 Envelope Detector

Envelope detectors are commonly used in direct-detection RF receivers. The envelope detector offers a low-power and simplified circuit technique for the signal down-conversion when compared to RF mixers and LO. This section discusses common schematic design of the RF envelope detectors that are used in WuRx. Figure 2.18 shows the schematic of the self-biased active RF envelope detector proposed in [17] .

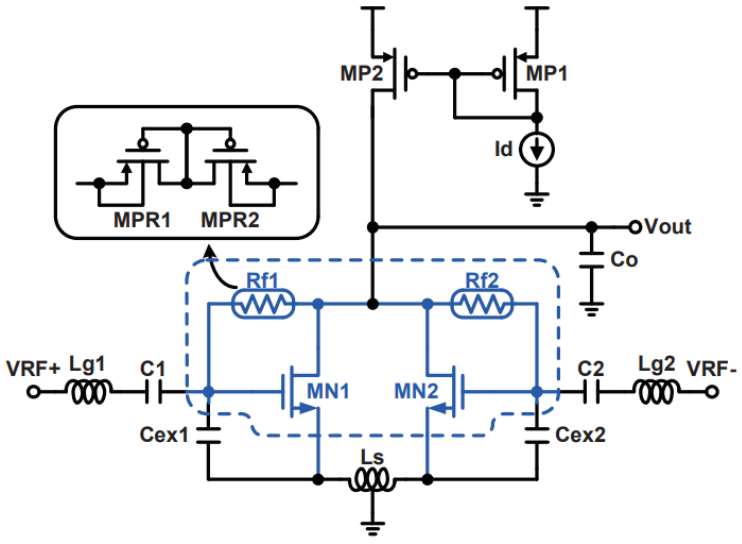


Figure 2.18: *Schematic of the self-biased active RF envelope detector [17]*

The large feedback resistor realized by a pseudo-resistor using MPR_1 and MPR_2 provides a DC biasing for the input differential transistors, in addition to an isolation between the input and the output. The RF detector input impedance matching provides a passive gain for the RF input signal. The gate inductors L_{g1} and L_{g2} are adjusted to allow the front-end to operate at two different frequencies of 2.4 and 5.8 GHz. The RF detector dissipates 1.5 µW, and provides significant sensitivity improvement when compared with classical RF envelope detectors based on Schottky diodes [12].

Another approach of direct-detection front-end is proposed in [18]. The FEA dissipates 48 µW allowing for high receiver sensitivity. The receiver FEA is shown in Figure 2.19, where it provides a precise input impedance matching, so that the input signal voltage swing is maximized at the frequency of interest and overcomes the noise of the subsequent envelope detector stage. The receiver antenna is directly connected to a narrowband BAW and capacitors transformer (C_1, C_2). The capacitors match along with the BAW at resonance frequency to 50 Ω resistance of the receiver antenna. The transistors M_1 and M_2 form a cascade amplifier with an active inductive load realized by M_3, M_4 and M_5. The envelope detector is connected directly to the FEA, which is realized using MOS version of the proposed peak detector in [34].

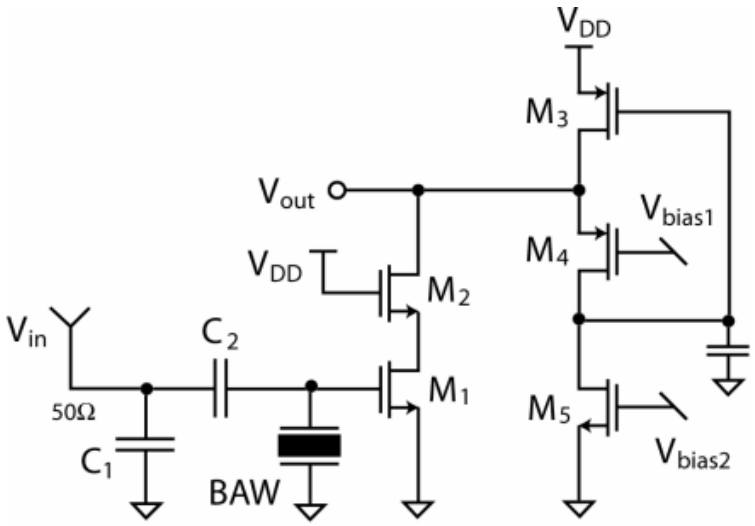


Figure 2.19: *Front-end amplifier schematic with input impedance matching [18]*

The receiver front-end schematic of the proposed WuRx in [19] is shown in Figure 2.20. The SAW filter has a narrow bandwidth of 11 MHz to remove out-of-band interferers and noise. The off-chip high-Q factor inductors L_1 and L_2 are used to provide 50 Ω input impedance matching. The input transistor P_1 operates in weak-inversion region and dissipates an ultra-low-power. The first stage works as an active RF envelope detector and as a first gain stage of the baseband amplifier. The low-frequency gain is improved by the feedback transistor P_2 and the resistor R_3. The gain of the baseband amplifier is 30 dB and 3 dB bandwidth range from 100 Hz to 1.2 MHz, while dissipating 1.25 µW.

The envelope detector shown in Figure 2.21 is used in the multi-stage WuRx proposed in [21]. It is realized using series of Schottky rectifier stages. The absence of Schottky diodes biasing circuits result in an extreme low-power detector. The rectified voltage is used to toggle the CMOS inverters. Additionally, a biasing circuit is added to the inverters

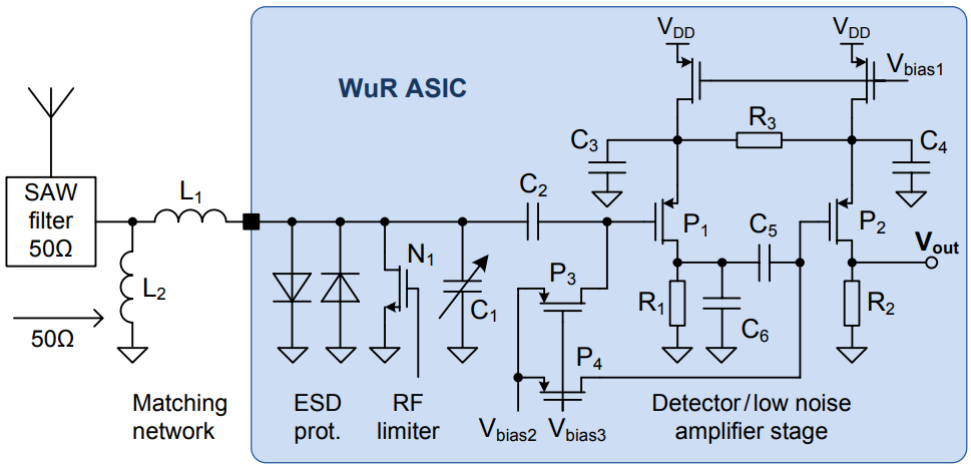


Figure 2.20: *Receiver font-end schematic [19]*

to provide switching point near to the switching threshold. The input impedance of the RF rectifier is high, making it hard to match it to 50 Ω receiver antenna, which results in a poor receiver sensitivity.

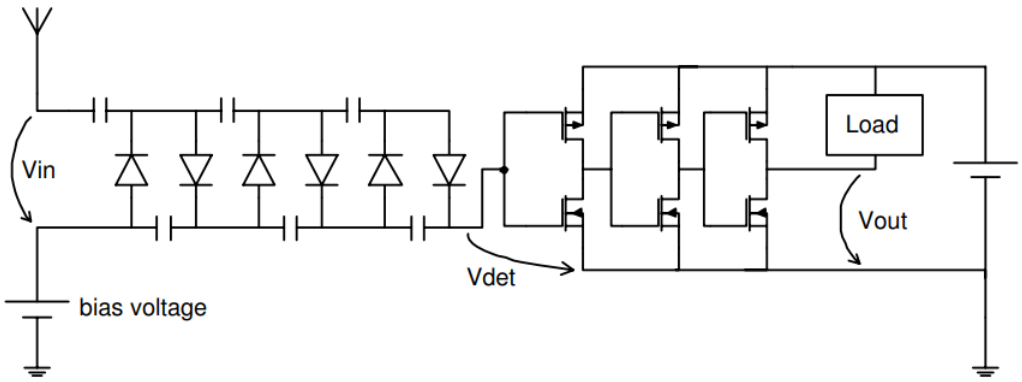


Figure 2.21: *Schematic of the RF detection front-end [21]*

2.3.5 Passive Circuits

Passive circuits, where no supply voltage source is used, are used in low-power RF radio designs. The proposed RF envelope detectors in [35], [36] are used in direct-detection WuRx design. The schematic of the passive RF envelope detector is shown in Figure 2.22. The RF detector is based on Dickson topology, where each stage consists of series of diodes realized in NMOS arranged in parallel to the input RF signal. At each stage output, the output capacitor stores the rectified signal. Four parameters are considered in the design. The Open-Circuit Voltage Sensitivity (OCVS), which defines the ratio between the rectified DC voltage and the square of the input RF signal. The rectified output increases linearly with the number of used stages. The charge-time or the time required for the signal to rise from 10 % to 90 % defines the detection data-rate, and hence keeping the charging-time to the minimum is desired. The third design parameter is the input

impedance, which is considered at zero bias of all the diodes in shunt. With each additional Dickson stage, the total shunt resistance seen at the input R_{in} is decreased, while the shunt capacitance is increased. The last parameter is the output noise. Since the diodes operate in zero biased, there is no noise source other than the thermal noise. The passive RF envelope detector is an attractive approach for low-power detection, however to increase the sensitivity, multiple stages are required, which increase the detection charging-time, making it unsuitable for micro-seconds WuRx response time.

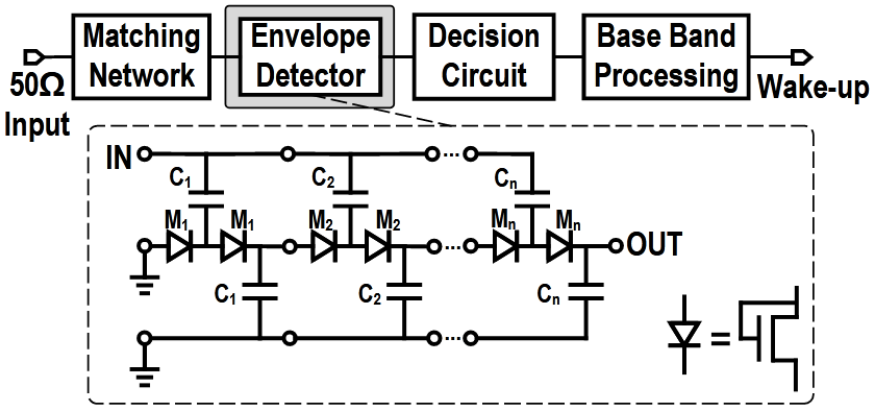


Figure 2.22: *Multi-stage passive RF envelope detector based on Dickson topology [35]*

Another passive circuit that is used in RF transceivers is proposed in [33]. The RF mixer circuit shown in Figure 2.23 is a passive circuit that is used in signal up and down conversion. The transistors are operating as switches controlled by the LO signal. The circuit is comparable to Gilbert cell operating principle, however there is no voltage-to-current conversion. Since the passive RF mixer has no conversion gain and high NF, the signal amplitude loss is compensated in subsequent circuits.

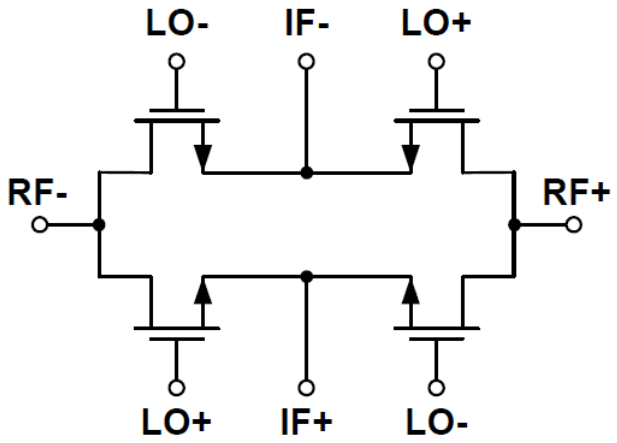


Figure 2.23: *Transistor ring passive RF mixer [23]*

2.4 CMOS Technology

Because of its low-power and high speed, CMOS technology has been widely used in digital IC design. The rapid down-sizing of the transistors and the complementary logic structure, makes the CMOS technology most suitable for high-density and large digital circuits. CMOS technology has not been used in analog and RF circuit design, since it was assumed to have degraded performance if compared to silicon bipolar technology [37]. CMOS technology scaling has improved several parameters that made it suitable for analog and RF circuit design, such as the MOSFETs transit frequency f_T, the device matching and minimum NF, in addition to its low-power and size [38]. The improvement of these parameters make it a suitable approach for RF analog design, especially for low-power applications. The set of technology parameters used to represent the digital technology are inadequate for RF analog design. Using CMOS technology in RF analog circuits requires accurate device modeling and characteristics optimization, especially in the sub-micrometers technologies. For example, in oscillators design, if the passive components such as capacitors and inductors do not have accurate model for their parasitics, process variation and temperature dependency, a significant deviation in the output frequency is produced.

2.4.1 Characterization for Analog Design

For RF and analog circuit design, several device characteristics have to be accurately modeled in SPICE device model. The most important device characteristics are briefly discussed in this section. For more details refer to [37]–[39]:

- **DC and AC behaviour:** the MOSFET I_D - V_{DS} characterization reduces the overall error in the curve fitting procedure. SPICE model uses many parameters to lower such errors. For precise (I_D - V_{DS}) curve, several measured points of (V_{GS}-V_{TH}) and I_D are considered in the model. For AC behaviour, the AC characterization needs to be considered on the device and on the circuit levels. The device f_T and f_{max} are considered on several DC MOSFET biasing points. For AC characterization on the circuit level, testing blocks such as oscillators and comparators are used to extract the AC behavior, where the complexity and information obtained from the circuit plays a significant role in understanding the device AC behavior. In addition, the correlation between the test circuit speed and process corners, helps to define a reliable behavior under process variation.
- **Linearity:** in passive elements, such as resistors and capacitors, the linearity is characterized with respect to the voltage across their terminals. The potential difference is modeled using Taylor expansion that equals to $x \approx (1 + \alpha_1 V + \alpha_2 V^2)$. The value of α_1 and α_2 are measured for different types of passive elements within the process, where they play a significant role in defining their linearity. For the active devices, the linearity is characterized on the circuit-level, using test circuits such as differential Op-Amps. The input linearity is measured by applying differential input voltage and observing the output short-circuit current, where the voltage is constant. Vice versa, the output linearity is measured by setting the input voltage to zero and observing the output large-signal impedance.

- **Device matching:** the physical matching of the active and passive devices in term of dimensions and process constants plays a significant role in RF analog design, especially in narrowband applications such as oscillators and RF amplifiers. In addition, the devices mismatch must be accurately included in the device models, so that during the circuit design phase, the mismatches are simulated and well considered.
- **Temperature dependency:** the effect of temperature variation on devices parameters are considered in the process models. The device charge mobility, sub-threshold conductance and capacitance are examples of device parameters that are affected by temperature variations. For low-power circuit design, the transistors which are biased in sub-threshold region are significantly influenced by temperature variation.
- **Noise:** thermal, flicker $1/f$ and other types of noise characteristics are included in the devices SPICE model. Based on measurements, it is difficult to measure the values of the noise since they are small. For that, testing circuits such as amplifiers are used, but their own contribution is sufficiently smaller than the Device Under Test (DUT).

2.5 Co-channel Interference Robustness

In addition to low-power dissipation design objective in WuRx, exhibiting a co-channel interference robustness is desired. Improving co-channel interference robustness in WuRx using coherent detection and highly linear RF devices (i.e LNA, RF mixers and LO) is avoided due to its significant increase of power dissipation. The approach in [40], proposes a robust wireless communication system based on SAW delay lines. The SAW delay line is a passive device fabricated using piezoelectric materials. In the proposed approach, the communication modulation is based on the LFM. The SAW correlator detects the LFM signal, which operates at 438.8 MHz with a bandwidth of 80 MHz. The SAW correlator operates as a Matched Filter (MF), and is able to detect the incoming RF signal and generate an RF pulse at its output port, with improved output SNR and reduced sidelobes of -42 dB compared to the correlated peak signal. This mechanism provides a passive immunity against co-channel signals, since the SAW correlator provides only the maximum sidelobes difference for specific incoming signal scheme, which in this approach is the LFM signal, while co-channel signals are suppressed by the device IL. Another approach based on BPSK SAW correlator is presented in [41] and shown in Figure 2.24. The approach increases the SNR of passive tags using 5-bits Barker-coded BPSK RF signal. The SAW correlator works at 100 MHz and is fabricated on Lithium Niobate $LiNbO_3$ substrate. When the SAW correlates with 5-bits Barker coded signal, 19.3 dB improvement in the device output SNR is achieved. The perfect correlation and the maximum compression gain is achieved when the SAW correlator structure is the time-reversed version of the excitation signal. Otherwise partial or no correlation is achieved, making this working mechanism an attractive approach for co-channel signals suppression.

The SAW correlator is used in direct-detection receivers as proposed in [42]. The SAW correlator works as a signal processor at GHz frequencies. Figure 2.25 shows the proposed direct-detection receiver. The wideband SAW correlator is fabricated on Lithium

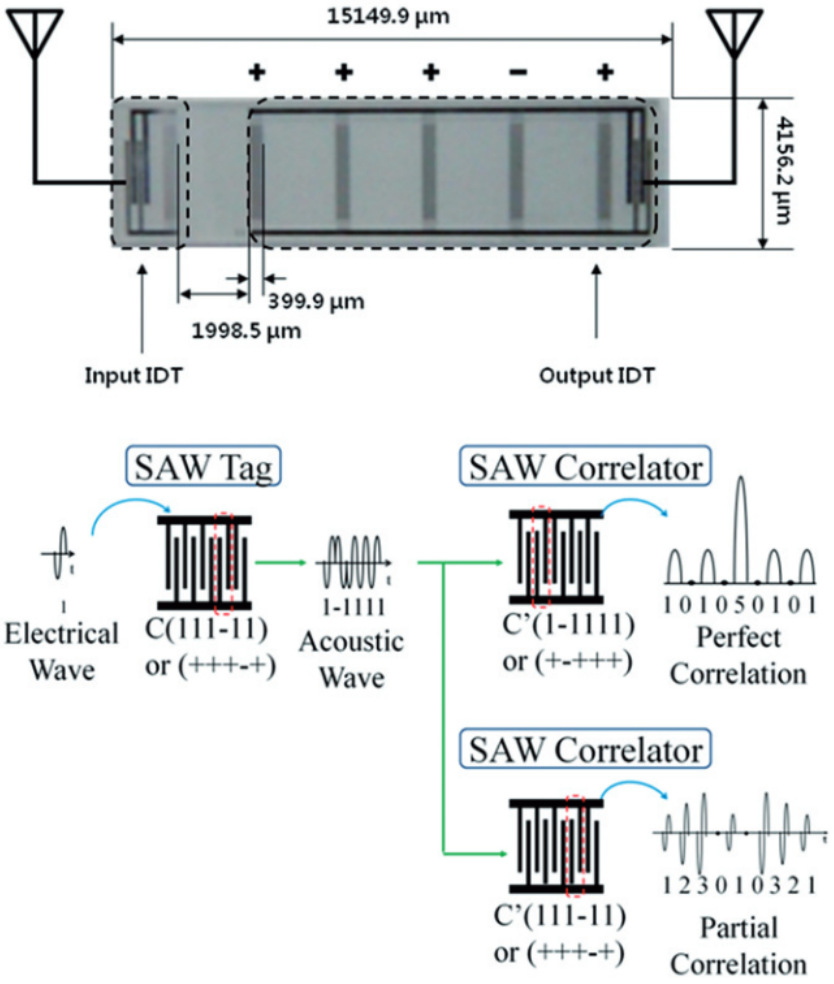


Figure 2.24: *5-bits Barker-coded SAW correlator substrate (upper figure) and the signal correlation output [41]*

Niobate $LiNbO_3$ substrate and works at 915 MHz, 2.43 GHz and 5.6 GHz with 1.25 %, 3.3 %, 12.5 %, 25 % and 50 % fractional bandwidths. The SAW correlator operates as a pulse compressor for the BPSK RF input signal. The output pulse peak-to-sidelobe difference is 31 dB and the device IL is 20 dB. The output pulse is amplified by an LNA and then detected by an RF envelope detector, where it is converted to baseband signal and subsequently amplified by the baseband amplifier.

The proposed approaches in this section use the SAW correlator (either based on LFM or BPSK modulation) as an RF passive signal processing stage, that is later detected and converted to baseband signal. These approaches offer a mechanism for generating a compressed pulse with specific peak-to-sidelobe difference, while suppressing other signals that do not match with the SAW correlator structure. With this working principle, a passive approach for co-channel interference robustness is achieved. However, the SAW devices exhibit a high IL, which reduces the receiver sensitivity.

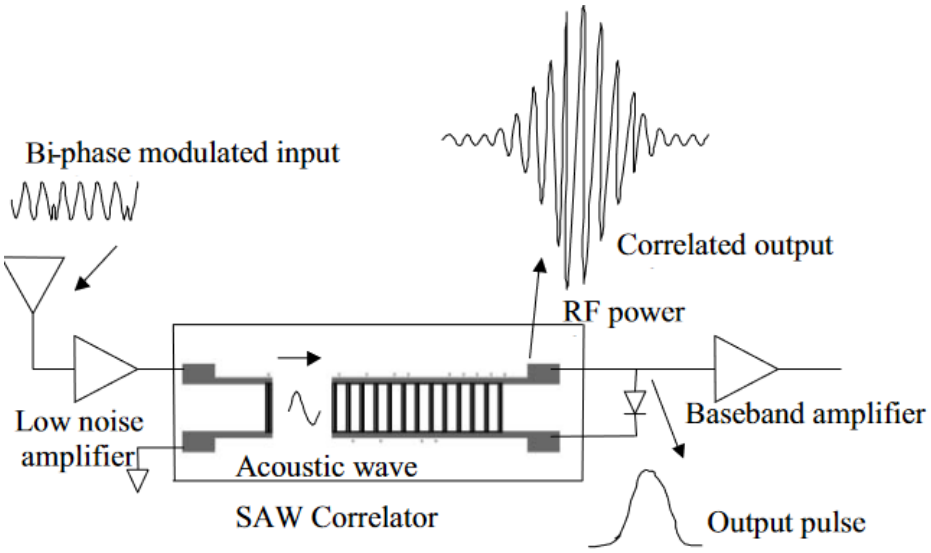


Figure 2.25: *SAW correlator based RF to baseband receiver [42]*

2.6 Proposed WuRx Architecture

Low-power dissipation is the most important design requirement in the WuRx design. Direct-detection receiver architecture provides a low-power dissipation and minimizes the design hardware complexity. Figure 2.26(a) shows the basic blocks of direct-detection receiver. The direct-detection receiver is a non-coherent receiver that has a BSF, followed by a demodulation circuit, which uses an RF envelope detector. The RF envelope detector converts the received RF signal to baseband signal. The absence of LNA, RF mixers and LO makes the direct-detection scheme a suitable candidate to operate at low-power dissipation levels.

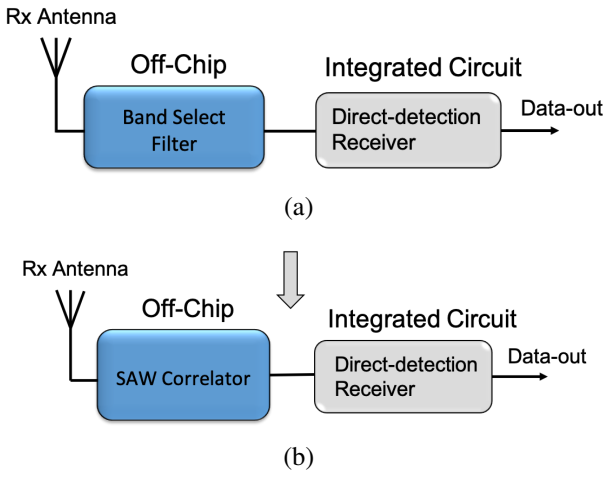


Figure 2.26: *(a) Conventional direct-detection receiver architecture (b) Direct-detection receiver with SAW correlator*

However, wireless receivers that use pure direct-detection suffer inevitably from co-channel interference due to the non-coherent receiver scheme. This degrades significantly the reliability of the WSN in unlicensed frequency bands. Therefore, a WuRx must not only

be power-efficient, but also robust to co-channel interference. In RF receivers, co-channel interference robustness is usually achieved using coherent receivers (heterodyne or homodyne) and narrowband filtering. However, this method requires highly linear RF amplifiers and RF mixers as well as a LO, leading to high levels of power dissipation. As mentioned in this chapter, to improve the receiver co-channel interference robustness, which is considered an important WuRx design parameter, an RF input signal pre-processing passive stage is proposed by means of an SAW correlator. The SAW correlator is a linear and passive RF signal processing element. The SAW correlator provides compression gain for specific received RF signal scheme, while suppressing other in-band signals. Figure 2.26(a) shows the block diagram of a conventional direct-detection receiver with BSF, while Figure 2.26(b) shows the proposed receiver architecture using an SAW correlator. The RF front-end consists of an SAW correlator followed by an RF envelope detector. Both are utilized to demodulate and detect the received RF signal and convert it to a baseband signal. SAW correlators exhibit significant device IL, which depends on the material used and device size, leading to a degradation in the receiver sensitivity [8], [A1]. Increasing the receiver sensitivity and communication range are design requirements that need to be met in the presence of the high SAW device losses. Due to the large baseband bandwidth in direct-detection receivers, the receiver sensitivity is further reduced. Reducing the baseband bandwidth by means of an NBC improves the receiver sensitivity on the expense of reducing the communication date-rate [A2], [40]. Depending on the application of the WSN, the wake-up time varies. Maintaining a WuRx response time in order of μs is also an important WuRx design parameter, which makes it suitable to be integrated in wide range of WSN applications. The size of the WuRx IC is other design requirement, where maintaining small WuRx IC size makes the integration in WSN nodes easier.

The proposed WuRx architecture is shown in Figure 2.27. The receiver has an off-chip part and an WuRx IC implemented in CMOS TSMC65n technology. In addition to the digital processing part.

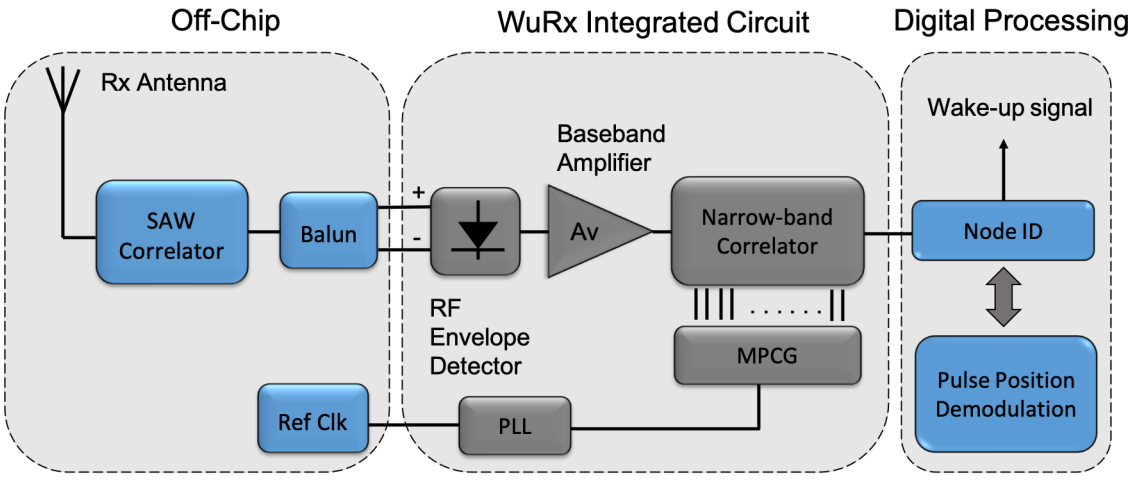


Figure 2.27: *Proposed WuRx block diagram*

The off-chip part is composed of an omni-directional antenna, with gain ranges from 2 – 3 dBi. The antenna is followed by an SAW correlator, which is a passive device that pre-processes the receiver RF signal. The SAW correlator provides a passive mecha-

nism of co-channel interference robustness [A5]. The SAW is followed by an RF balun, since the inputs of the proposed RF envelope detector are differential. The low-power RF envelope detector detects and down-converts the correlated signal coming from the SAW correlator. The RF envelope detector is a non-coherent detector that converts the RF signal to a baseband signal. Both the SAW correlator and the RF part of the envelope detector represent the receiver front-end. The baseband signal is further amplified by a low-power baseband amplifier, that amplifies the baseband signal to an appropriate level for further processing. Due to the high baseband bandwidth, the baseband amplifier is followed by an NBC, that reduces the baseband signal bandwidth, resulting in an increase in the total receiver sensitivity. The NBC is a parallel Integrate and Hold circuit (IHC) that accumulates the detected baseband signal and extracts the same information, but with reduced baseband bandwidth and communication data-rate. For this purpose, it needs to be driven by a low-power Multi-Phase Clock Generator (MPCG) that generates multiple clocks, which are equal to the number of the parallel IHCs units. Each generated clock has constant time-phase. With this technique, there is no need to make synchronization between the base station and the WuRx. The input clock of the MPCG comes from a low-power PLL that has an external quartz oscillator as a reference clock. The Node ID is demodulated using a Pulse Position Demodulation (PPM) technique, which is buffered in the node registers to be later compared with the pre-configured node ID. If the received ID matches the node stored ID, a wake-up signal is asserted, otherwise not. Detailed design of the WuRx components is discussed in Chapter 4.

2.7 Summary

In this chapter, an exploration of the related state-of-art WuRx architectures, circuit design techniques, co-channel interference robustness and technology is carried out. In addition to the proposed WuRx architecture that is designed, fabricated and measured in this thesis. From the fundamental RF receiver architectures, one concludes that coherent receiver architecture achieves high receiver sensitivity and co-channel interference robustness, but it is not a suitable approach for the WuRx design due to its high power dissipation, which mainly comes from the RF amplification stage, the down-conversion circuit and the LO. Three basic working scheme of the WuRx are discussed, with more focus on the always-on scheme. The always-on WuRx working scheme provides an on-demand and asynchronous working scheme in WSN. However, since it is in always-on state, the low-power dissipation level represents the major design challenge compared with the other two WuRx working schemes.

Operating in weak-inversion region represents an attractive approach for WuRx, but careful design and corners simulation should be considered. Reducing the power supply in WuRx reduces the power dissipation at the expense of reducing the RF performance, which is undesired. The current-reuse is used in low-power receivers, however, the power dissipation reduction is not insignificant, and hence the power dissipation design target is not achieved. The active RF envelope detector presents a suitable approach for low-power receiver design, however it trades-off power with poor sensitivity and high baseband bandwidth. Passive circuits are used in direct-detection receivers, but achieves poor sensitivity and slow response time.

As discussed in the proposed WuRx architecture section, a direct-detection-based WuRx presents a suitable architecture for low-power WuRx, however, due to its wide baseband bandwidth, the direct-detection receiver sensitivity is poor. The receiver sensitivity can be improved by reducing the baseband bandwidth, trading-off the sensitivity with the data-rate. To improve the co-channel interference robustness, a passive design technique based on off-chip SAW correlator is proposed. The SAW correlator provides a compression gain for specific signal schemes, such as the LFM and BPSK signals, while other in-band signals are attenuated. The SAW correlator represents an attractive approach to be used in WuRx, however, achieving enough compression gain is highly dependent on the device size, which results in higher IL. In addition the power compression gain is affected by factors such as the fabrication capabilities, the material and the electro-mechanical coupling.

3 System Level Analysis and Design

A detailed WuRx system-level analysis is demonstrated in this chapter. The analysis starts with defining the WSN design considerations and challenges, given that the WSN is considered the application domain of the WuRx. Subsequently, a detailed system analysis of the SAW correlator is presented. The analysis explains the device operating principle, modeling techniques and design parameters. The definition of the device modulation scheme and physical parameters helps in the device parameters selection and fabrication feasibility. The chapter ends with analysing the WuRx communication performance, such as the receiver sensitivity and the communication range, in addition to the WuRx chip design target.

3.1 Design Considerations of Wireless Sensor Networks

Maintaining reliable WSN functionality requires careful design optimization in the network, sensing node structure and communication scheme. This section defines the WSN design considerations, challenges and constraints that need to be met when designing a WSN.

3.1.1 Basic WSN Characteristics

- **Extended Node Lifetime**: as mentioned in Chapter 1, the WSN nodes are powered-up with batteries, which provide a limited power budget. Increasing the nodes operating lifetime is a significant design characteristic, making the low-power WSN node design constraint a primary design objective. Due to the fact that WSN nodes are geographically distributed in a potentially wide area, periodic battery replacement or maintenance is expensive and not a practical solution [2].
- **Communication Performance**: increasing the communication range between the base station and the WSN nodes, or between two sensor nodes requires an increase in the transmitted average power. On the receiver side, and as discussed in Section 2.1, high receiver sensitivity and co-channel interference robustness are achieved using highly linear RF amplifiers, mixers and LO, which leads to high levels of power dissipation [10]. Improving receiver sensitivity and co-channel interference robustness increases the communication distance and reliability. The speed of data collection and communication are considered an important WSN design parameters. Depending on the WSN application, the communication delay is defined within a specific time constraint. In real-time applications, real-time data collection is required, while in soft-time applications, increased delay response is tolerated [2].
- **High System Integration**: the WSN node is composed of several components such as sensors, Analog-to-Digital Converter (ADC), communication interfaces, processor and transceiver. Maintaining a compact design, with high system integration

facilitates installing and removing WSN nodes [2], [6]. In addition, it provides robustness against harsh environment, which protects the node from damage and increases its operation lifetime.

- **Scalability and Node Cost**: WSN nodes are usually deployed in large numbers and cover large geographical area. Therefore, the WSN exhibits flexibility in adding/discarding any number of nodes without affecting the network operation. Additionally, due to the large number of nodes used in the WSN, maintaining low-node cost is preferred.
- **Flexibility and Adaptability**: the WSNs and nodes are configurable to achieve the optimal performance, when there is a change in the network location and topology. The WSN nodes have multiple modes of operation that determine the power dissipation, such as active or sleep-mode. In addition, WSNs operate at different frequencies or data-rates depending on the targeted application and operating scenario [2].

3.1.2 Single-hop Versus Multi-hop Communication Scheme

Single-hop communication scheme consists of single base station or single hub point connected directly to the network nodes. The Star WSN topology shown in Figure 3.1(a) is a common example of the single-hop communication scheme. The nodes are connected at different communication range, so the transmission range and sensitivity are sufficient to maintain a direct data transmission with a single-hop communication from the sensor nodes to the base station [2], [6]. The Star topology is simple to implement and flexible to network extension. However, failure in the base station results of a failure in the entire network. In addition, the WSN covers a large geographical area, which makes the single-hop a non-practical network structure. The multi-hop communication scheme is similar to the Star topology, however the nodes are not only connected directly to the base station, but through other nodes. These intermediate points work as aggregation nodes as shown in Figure 3.1(b). In multi-hop communication scheme, the sensor node does not only exchange data with the base station, but also serves as relay for other sensor nodes, where aggregation nodes collaborate to transfer data from other nodes to the base station through a multi-hop path from the desired node to the base station. The multi-hop communication scheme is used to cover large geographical area, beside keeping the communication power between the nodes to the minimum, making it a suitable candidate in low-power WSN design [2], [6]. However, failure in the base station results in a failure in the entire network, in addition if an aggregation node fails, the sensor nodes connected to this point fail as well, making the nodes failure in multi-hop communication scheme more severe than Star topology, in the case the failed node is an aggregation node, since it servers as a local base station.

3.1.3 Sensing Node Architecture

A sensor node is the basic building block of the WSN, where the sensing, data processing and communication take place. Figure 3.2 shows the basic building blocks of a wireless sensor node. The node consists of the following [2], [3], [6]:

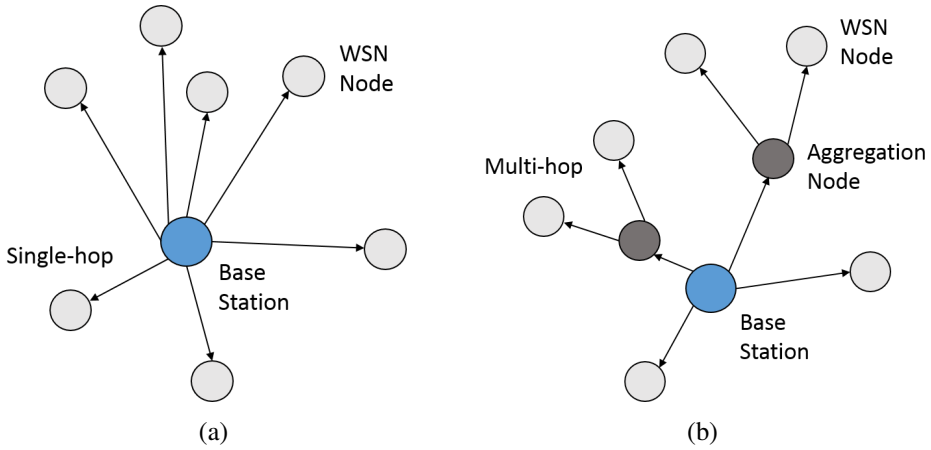


Figure 3.1: *(a) Single-hop Star communication scheme (b) Multi-hop communication scheme [2]*

- **Data Acquisition Subsystem:** it contains one or more physical sensors that sense and read physical quantities. The collected data is converted by an ADC and sent to the processing unit via I/O interfaces such as a Serial Peripheral Interface (SPI).
- **Processing Subsystem:** it connects other node subsystems together. The processing subsystem consists of a microprocessor, memory and a non-volatile flash memory. Depending on the application, the microprocessor processes the collected data, converts and sends it to the communication subsystem. The memory stores the running program instructions and the collected data. The flash memory stores the firmware and the running program instructions set permanently.
- **Communication Subsystem:** it consists of the communication transceiver and antenna. The communication subsystem is considered the most power hungry subsystem, where it dissipates most of the power budget of the WSN node.
- **Power Unit:** it provides the needed electrical power to the node. Depending on the application and node lifetime, the power unit capacity varies from one node to another.

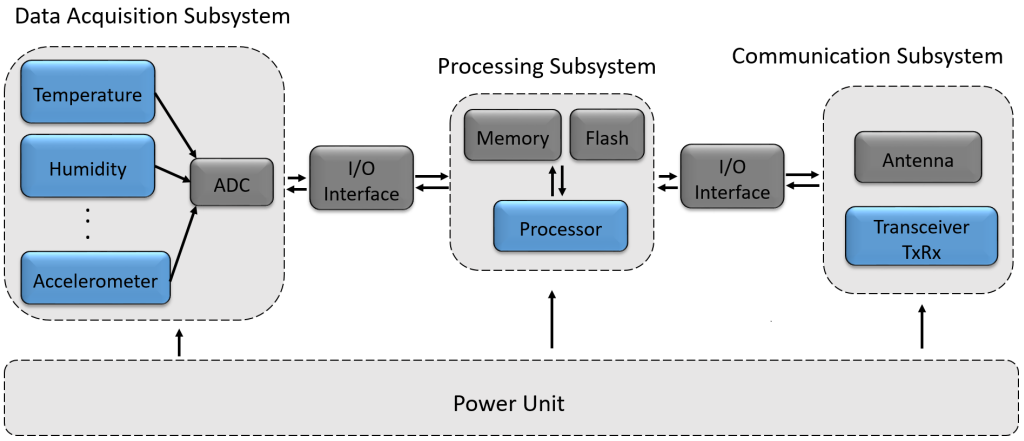


Figure 3.2: *Basic architecture of WSN node [3]*

3.1.4 Challenges and Constraints of Network and Node Design

- **Low-Power Dissipation:** minimizing static and dynamic node power dissipation results in longer node lifetime and decreases the WSN failure due to energy source depletion. As mentioned in Chapter 1, reducing the power dissipation is achieved by the communication scheme (duty-cycle communication protocol) [2], [3], or using hardware techniques such as energy harvesting or asynchronous communication by means of WuRx [A5], [40].

- **Self-organizing:** in many WSN applications, the sensor nodes operate in harsh environment without technical support and maintenance. As a result, the sensors are designed to be able to change their configurations [2]. Self-organizing of sensor nodes includes the node ability to perform self-optimization by selecting its own configuration, such as the preferred communication frequency and bandwidth, in addition to the proper transmission power to maintain reliable communication. Self-healing and protection are other requirements for self-organizing of sensor nodes. The self-healing is defined as the ability of the WSN to stay functional as a result of a failure such as energy source depletion, hardware breakdown or failure in communication links. Self-protecting is the ability of the sensor nodes to block and work against security attacks [2], [3].

- **Security:** the broad applications spectra from manufacturing, transportation, military to scientific research make the network security an essential design challenge [6]. As an example, Jamming attack over sensor nodes is a known security threat that results in a DoS in the network. As a solution for radio jamming, sensor nodes switch to other communication technique such as optical rather than radio. Such solution increases the node design complexity, power dissipation, cost and size [2], [6].

- **Quality of Service (QoS):** measures the WSN performance. Fulfilling QoS parameters ensures efficient and reliable information transmission. QoS measures include data-delay, jitter, bandwidth and Bit Error Rate (BER). The constraints over QoS parameters vary in network applications, as some applications tolerate data-delay or falsely signal, while others not [A5], [40], [43].

3.2 Surface Acoustic Wave (SAW) Correlator

The SAW correlator is the first component in the proposed WuRx following the receiver antenna as shown in Figure 2.27. It is proposed in the WuRx design to provide a passive detection of the input RF signal, making it a reasonable approach in low-power receivers design. In this section, the basic working principle and applications of SAW devices are discussed. Furthermore, based on a feasibility study from [8], [9], a detailed analysis for the SAW device criteria such as frequency, modulation schemes, material and fabrication feasibility is demonstrated. The feasibility study is used to decide which device is suitable in the WuRx design. The last section discusses different modeling techniques and levels for the SAW devices.

3.2.1 Principle and Applications

Surface Acoustic Waves, also known as (Rayleigh waves) are a type of longitudinal waves that propagates along an elastic solid surface such as piezoelectric substrate. The SAW was discovered in 1885 by Lord Rayleigh and named after him. The piezoelectric phenomenon has a wide spectrum of applications in the field of signal processing and wireless communication, which operate at frequencies ranging from 10 MHz to several GHz . In recent years, the SAW devices are frequently used in the Industrial, Scientific, and Medical (ISM) frequency band, as well as in intermediate frequency devices for circuits operating at higher RF frequencies [44]. The SAW devices are realized as Band Pass Filters (BPF), Matched Filters (MF), Delay-lines, resonators and correlators. The commonly used piezoelectric substrates are Quartz, Lithium Niobate ($LiNbO_3$), Lithium Tantalate ($LiTaO_3$) and Gallium Arsenide ($GaAs$). Each substrate has different material properties such as the wave propagation velocity, the coupling coefficient, the device IL and the temperature dependency [45]. The basic structure of the SAW device is shown in Figure 3.3. It consists of two Inter-Digital Transducers (IDTs), which are thin-metal films mounted on the surface of the piezoelectric substrate. The first IDT is located at the input of the SAW device, while the second one is at the output port. Each IDT consists of several interleaved metal electrodes, which are used to receive and transmit the acoustic waves. The input IDT converts the applied electrical signal on the input port to a mechanical acoustic wave, which travels with specific wave velocity along the substrate surface. The SAW mechanical vibrations are converted back by the output port IDT to an electrical signal [45].

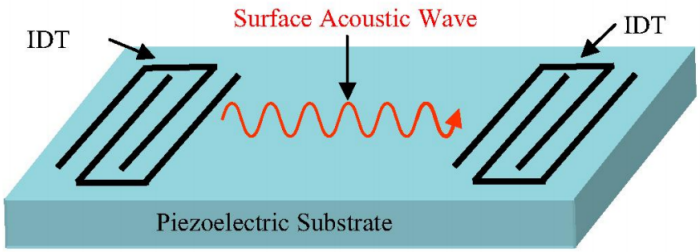


Figure 3.3: *Basic SAW device structure [46]*

The acoustic waves travel with velocity that depends on the piezoelectric material used and its geometry. Table 3.1 shows different substrate types, with their cut orientation and acoustic wave propagation velocity [45], [46]. From Table 3.1, the IDT period is defined as $\lambda = V/F$, where V is the acoustic wave propagation velocity and F is the device operating frequency. The piezoelectric effect is the production of an electrical signal due to a mechanical stress on the material substrate. When an electric source at specific frequency is applied to the input port of the SAW device, an electric field is formed in the gaps between the input port IDT, resulting in an acoustic wave generation due to the piezoelectric effect. If the input signal frequency has the same wavelength as the IDT period, all the acoustic waves are in-phase and therefore reinforce each other. As a result, a longer IDT provides a larger acoustic wave amplitude. The IDT on the output port has the same structure, but it is used to receive the acoustic waves and convert them back to electrical signal, in which its amplitude is a function of the IDT finger pairs arrangement and number [45].

Table 3.1: *Propagation velocity of different Piezoelectric orientation and substrates [44]*

Piezoelectric Substrate	Orientation	Velocity m/s
Quartz	ST X	3158
$LiNbO_3$	YZ	3488
	$41°rotYX$	4780
	$128°YX$	3980
$LiTaO_3$	$36°YX$	4220

3.2.2 Device Modulation and Parameters Selection

As shown in the proposed WuRx architecture, the robustness of WuRx against co-channel interference is improved by means of a passive pre-processing stage for the input RF signal. The RF signal pre-processing stage functions as a pulse compressor. The pulse compression is the process of converting long low-power signal into a narrow-pulse signal with high instantaneous power as shown in Figure 3.4. The output signal is a compressed pulse, which ideally has the same energy as the input low-power RF signal. In SAW pulse compressors, the input low-power signal correlates with the SAW device impulse response. The SAW device output SNR is increased if the input excitation signal matches the SAW device impulse response, while co-channel interferers and noise are suppressed. The SAW pulse compression systems are designed to be able to detect LFM input signals, which are also called up- or -down chirp signals, or detect BPSK signals, such as Barker-coded modulated signals. Factors such as frequency, compression gain, device material, coupling factor, temperature dependency, device size and fabrication feasibility play a significant role in deciding which device is appropriate to be used in the WuRx design [8], [9].

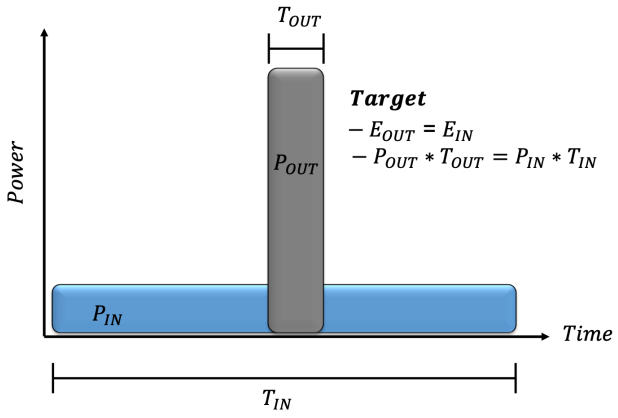


Figure 3.4: *Pulse compression principle*

Based on the feasibility study from [8], [9], two different SAW frequencies were considered for design and fabrication: 868 MHz with 2 MHz bandwidth and 33 dBm of average transmitted power, and 2.44 GHz with 80 MHz bandwidth, and 20 dBm of average transmitted power [47].

LFM Based SAW Correlator

The LFM scheme is a modulation scheme in which the signal frequency varies linearly with time as shown in Figure 3.5.

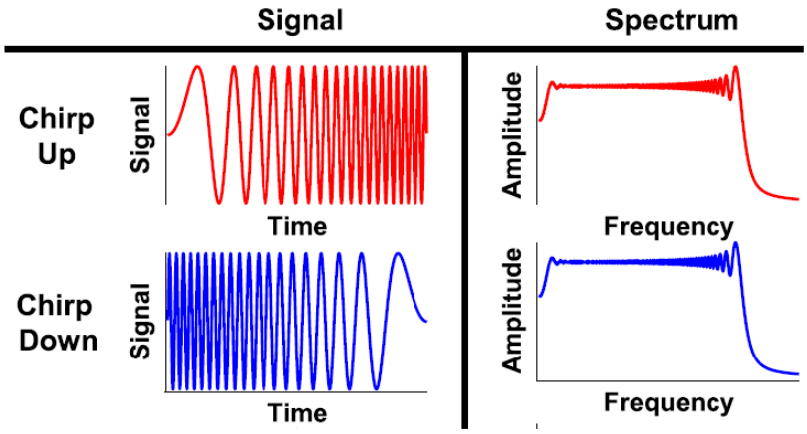


Figure 3.5: *Up- and down- chirp signals [48]*

The LFM signal is expressed in Equation (3.1).

$$x(t) = A(t)\cos(\theta(t)) \tag{3.1}$$

where A(t) is the chirp signal amplitude, which equals to zero outside the LFM signal wavetime T. The chirp instantaneous frequency is given in Equation (3.2).

$$f(t) = \frac{1}{2\pi}\frac{d\theta(t)}{dt} \tag{3.2}$$

The instantaneous frequency variation rate is expressed as:

$$\mu(t) = \frac{df(t)}{dt} = \frac{1}{2\pi}\frac{d^2\theta(t)}{dt^2}$$

If $\mu(t) > 0$ then the waveform is called up-chirp signal, while if $\mu(t) < 0$ then the waveform is down-chirp signal. When a chirped signal passes through an SAW device whose impulse response is also a chirp waveform, but with frequency sweeping in the opposite direction, the output is an RF peak at the chirp center frequency. Where the RF peak period is smaller than the wavetime T and equals to $1/(B\text{x}T)$, where B is the chirp bandwidth. The compression capability is characterized by the power compression gain, which equals in LFM signal to $B\text{x}T$ [40].

Case 1: consider an LFM based SAW correlator operating at 2.4 GHz with 80 MHz bandwidth detecting an LFM input RF signal at 2.4 GHz with 1.25 µs wavetime. This configuration results in a power compression gain of $B\text{x}T = 100$, which equals to the device output SNR improvement. From the device IL perspective, the $LiNbO_3$ substrate has 1 dB/µs at 1 GHz, and it grows proportional to the square of the device frequency and reaches to 5.7 dB/µs at 2.4 GHz. On the other hand, the IL is three times higher in quartz substrate operating at higher frequencies such as 2.4 GHz making the quartz substrate not

a suitable material for LFM based SAW correlator at 2.4 GHz fabrication. The coupling factor K^2 in $LiNbO_3$ ranges from 7% to 10%, while in Quartz, it is 0.1%. Based on the acoustic wave velocity of the 128°YX substrate of 3980 m/s and the input LFM signal wavetime of 1.25 µs, the device length is approximately 5 mm. From the fabrication feasibility perspective, making an LFM based SAW correlator at 2.4 GHz with 80 MHz bandwidth requires approximately 3048 periods (pairs of IDT), in order to cover the linear change of the signal frequency given that the SAW wavelength equals to 410 ps. The linear change in the IDT pairs wavelength is 80 MHz/3048 = 26.2 kHz, i.e the finger width change is about 4.33 pm, which is far beyond reach of any manufacturing technology used in SAW device fabrication [8], [9], [49]. Table 3.2 summarizes the parameters of 2.4 GHz LFM based SAW correlator, with their evaluation. The basic structure of the LFM based SAW correlator is shown in Figure 3.6, where the wavelength of the output port IDTs is increasing linearly:

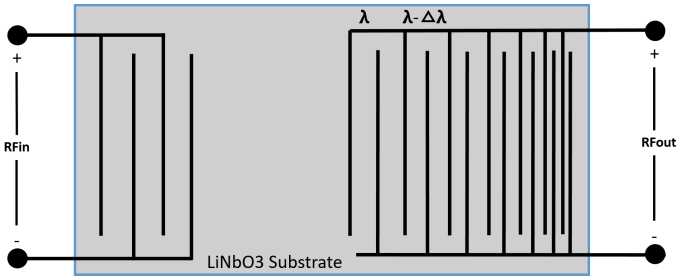


Figure 3.6: *Basic structure of the LFM based SAW correlator*

Table 3.2: *Feasibility parameters of LFM based SAW correlator at 2.4 GHz [8], [9]*

Parameter	**Value**	**Evaluation**
Power compression gain BxT	100 (20 dB)	++
Device size	Approx. 5 mm	+
Power losses in $LiNbO_3$ based device	5.7 dB	+
Coupling factor	7% to 10%	+
Temperature dependency	Variant	−
Number of IDT pairs	3048	−−
Change in finger width	4.10 pm	−−

Case 2: consider an LFM based SAW correlator operating at 868 MHz with a 2 MHz of bandwidth detecting an LFM input RF signal at 868 MHz with 1.25 µs wavetime. The device feasibility parameters are summarized in Table 3.3. After performing the same system analysis as in case 1, the small power compression gain is the main drawback of this approach. The compression gain is further improved by increasing the input signal wavetime, so the BxT product is increased, however this leads to a large device length, and hence more device power losses. In addition, the device configuration is also infeasible for fabrication due to the large number of IDT pairs [8], [9].

Table 3.3: *Feasibility parameters of LFM based SAW correlator at 868 MHz [8], [9]*

Parameter	**Value**	**Evaluation**
Power compression gain *BxT*	2.5 (4 dB)	−−
Device size	Approx. 5 mm	+
Power losses in $LiNbO_3$ based device	1 dB	++
Coupling factor	7% to 10%	+
Temperature dependency	Variant	−
Number of IDT pairs	3048	−−
Change in finger width	160 pm	−−

Barker Code Based SAW Correlator

Barker code is a set of digital sequences that alternates between logic one and zero. As an example, Figure 3.7 shows a 7-bits Barker-coded sine wave signal, where the signal phase changes with respect to the code sequence.

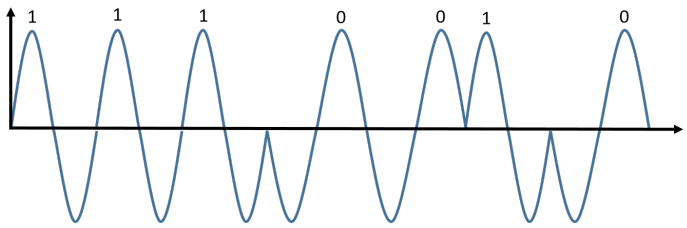


Figure 3.7: *7-bits Barker-coded BPSK sine wave signal*

If output port coded IDT pairs of the SAW correlator are designed with the reversed version of the input binary phased coded signal, then it results in a power compression gain, which is ideally equal to the length of the used Barker code sequence. For example, the 7-bits SAW correlator shown in Figure 3.8 has an output power SNR improvement equals to 7 (8.45 dB).

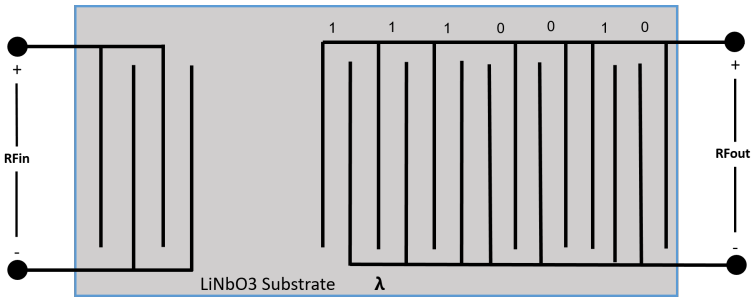


Figure 3.8: *Basic structure of 7-bits Barker code modulated SAW correlator*

Different Barker code sequence sets are shown in Table 3.4, with their corresponding power compression gain.

Case 1: consider a Barker-coded SAW correlator operating at 2.44 GHz with 80 MHz of bandwidth detecting a Barker-coded BPSK input RF signal at 2.44 GHz. The power compression is equal to the code length, and for 13-bits Barker-coded SAW correlator the

Table 3.4: *Barker code sequences, with their power compression gain for different Barker code length [8], [9]*

Code Length	Sequence	Power Compression Gain(dB)
2	1 0 or 0 1	3
3	1 1 0	4.7
4	1 1 0 1 or 1 1 1 0	6
5	1 1 1 0 1	7
7	1 1 1 0 0 1 0	8.45
11	1 1 1 0 0 0 1 0 0 1 0	10.4
13	1 1 1 1 1 0 0 1 1 0 1 0 1	11.1

output SNR improvement is 13 (11 dB). From the device size perspectives, it is obliged to have $T_0 = 1/B$ which equals to 0.125 µs, making a 13-bits SAW correlator length less than 1 mm, given that the $LiNbO_3$ substrate is used with SAW propagation velocity of 3980 m/s. The parameters evaluation is shown in Table 3.5.

Table 3.5: *Feasibility parameters of 13-bits Baker-coded SAW correlator at 2.44 GHz [8], [9]*

Parameter	Value	Evaluation
Power compression gain for 13-bits	13 (11.1 dB)	++
Device size	1 mm	+
Power losses in $LiNbO_3$ based device	5.7 dB	+
Coupling factor	7% to 10%	+
Temperature dependency	Variant	−
Number of IDT pairs	13	++
Change in finger width	0	++

Case 2: consider a Barker-coded SAW Correlator operating at 868 MHz with 2 MHz of bandwidth detecting a Barker-coded BPSK input RF signal at 868 MHz. The device feasibility parameters are summarized in Table 3.6 after performing the same system analysis as in case 1.

Table 3.6: *Feasibility parameters of 13-bits Baker-coded SAW correlator at 868 MHz [8], [9]*

Parameter	Value	Evaluation
Power compression gain for 13-bits	13 (11.1 dB)	++
Device size	20 mm	−−
Power losses in $LiNbO_3$ based device	1 dB	++
Coupling factor	7% to 10%	+
Temperature dependency	Variant	−
Number of IDT pairs	13	++
Change in finger width	0	++

Scheme and Frequency Selection: from the above feasibility analysis of the SAW device modulation schemes and parameters, the 13-bit BPSK Barker-coded SAW correlator at

2.44 GHz is selected for design and fabrication. The selected device modulation and parameters in Table 3.5 presents a trade-off between the correlator design requirements and the fabrication feasibility. Detailed design and simulation of the 13-bits Barker-coded SAW correlator is presented in Chapter 4.

3.2.3 Device Modeling Techniques

Several modeling methods are used to explain the operating principle of the SAW correlator. This section explains in details the mathematical model of the SAW correlator, and the analytical derivation of the device impulse response, demonstrating how the device increases the output SNR. In addition, the equivalent circuit model, which addresses the device electrical behaviors is presented. The Finite Element Modeling (FEM) is the last modeling technique, which is briefly mentioned, where it mainly explains the device operation, taking into account the physical device parameters.

Mathematical Model

The SAW correlator detects the input RF signal with a specific known waveform structure i.e Baker-coded signal or LFM. The SAW correlator is mathematically modelled as a MF, which is a linear filter that detects signals buried in noise. The MF increases the output SNR by providing a compression gain for the desired and known signal structure, while suppressing noise. The MF output is mathematically expressed as the convolution between the received signal $r(t)$ and its impulse response $h(t)$ as shown in Equation (3.3). The received signal is composed of the desired signal $x(t)$ and the input noise signal $n_{in}(t)$. If the received signal matches with the SAW correlator impulse response, then the result of the correlation process is an RF compressed pulse. Refer to [9], [A4] for more details about the mathematical analysis derivation.

$$r(t) * h(t) = x(t) * h(t) + n_{in}(t) * h(t) \tag{3.3}$$

The derivation of the SAW correlator impulse response $h(t)$ starts by defining the device output instantaneous $SNR_{out}(t)$, which is the ratio between the output signal power $P_{out}(t)$ divided by the output noise power $P_{noise}(t)$ as expressed in Equation (3.4).

$$SNR_{out}(t) = \frac{P_{out}(t))}{P_{noise}(t)} \tag{3.4}$$

For a correlator with a delay of t_d, the time-domain output is a compressed RF peak where the peak voltage is reached at a located time $t = t_d$. The $SNR(t_d)$ is the maximum SNR, and $t = t_d$ represents the optimal decision time when the output signal exhibits its maximum SNR. The impulse response $h(t)$ must be designed in a way that $SNR_{out}(t)$ is maximized to achieve the MF functionality of providing co-channel interference robustness and noise suppression. For a linear system and based on Equation (3.3), $y(t)$ which refers to the output signal components is defined as $x(t) * h(t)$, and n_{out} which refers to the output noise components is defined as $n_{in} * h(t)$. Based on Equation (3.4), the output peak SNR_{peak} is

expressed in Equation (3.5), where the peak output signal power is divided by the average output noise power. Equation (3.5) is further extended to be expressed in frequency-domain using inverse Fourier transform and the properties of convolution theory in the frequency-domain.

$$\frac{|y(t_d)|^2}{\overline{|n_{out}(t)|^2}} = \frac{\left|\frac{1}{2\pi}\int_{-\infty}^{+\infty} X(\omega)H(\omega)e^{j\omega t_d}d\omega\right|^2}{\frac{1}{2\pi}\int_{-\infty}^{+\infty} S_{in}(\omega)\,|H(\omega)|^2\,d\omega} \tag{3.5}$$

$X(\omega)$ and $S_{in}(\omega)$ are the input signal and noise in frequency domain respectively, while $H(\omega)$ is the device transfer function. The objective is to drive the transfer function $H(\omega)$ or the impulse response $h(t)$ that maximizes the output SNR of the SAW correlator. To do this, Schwarz inequality is used [50]. As given in Equation (3.6), if two complex functions $f(t)$ and $g(t)$ are integrable over a closed period $[a, b]$ then

$$\left|\int_a^b f(x)g(x)dx\right|^2 \leq \int_a^b |f(x)|^2\,dx \int_a^b |g(x)|^2\,dx \tag{3.6}$$

The equality is only valid if the two functions are written as $g(\omega) = Kf(\omega)^*$. Considering $f(\omega)$ and $g(\omega)$ as in Equation (3.7):

$$\begin{aligned} f(\omega) &= \left[\frac{X(\omega)}{\sqrt{S_{in}(\omega)}}\right] \\ g(\omega) &= \sqrt{S_{in}(\omega)}H(\omega)e^{j\omega t_d} \end{aligned} \tag{3.7}$$

and substituting Schwarz inequality in Equation (3.7) into Equation (3.6) gives

$$\frac{|y(t_d)|^2}{\overline{|n_{out}(t)|^2}} \leq \frac{\frac{1}{2\pi}\int_{-\infty}^{+\infty}\left|\frac{X(\omega)}{\sqrt{S_{in}(\omega)}}\right|^2 d\omega \frac{1}{2\pi}\int_{-\infty}^{+\infty}\left|\sqrt{S_{in}(\omega)}H(\omega)e^{j\omega t_d}\right|^2 d\omega}{\frac{1}{2\pi}\int_{-\infty}^{+\infty} S_{in}(\omega)\,|H(\omega)|^2\,d\omega}$$

The term on the right side of the numerator cancels with the denominator term as expressed in Equation (3.8). This taken-out term represents the device output noise, which is produced from the correlation between the device impulse response and input noise.

$$\frac{|y(t_d)|^2}{\overline{|n_{out}(t)|^2}} \leq \frac{1}{2\pi}\int_{-\infty}^{+\infty}\frac{|X(\omega)|^2}{S_{in}(\omega)}d\omega \tag{3.8}$$

Depending on Schwarz inequality for equal terms, where $g(\omega) = Kf(\omega)^*$, Equation (3.7) is rewritten as:

$$\sqrt{S_{in}(\omega)}H(\omega)e^{j\omega t_d} = K\left[\frac{X(\omega)}{\sqrt{S_{in}(\omega)}}\right]^*$$

This implies that the optimal SAW correlator transfer function is expressed as $H(\omega) = X(\omega)^* e^{-j\omega t_d}$ with a corresponding impulse response equals to $h(t) = \tilde{x}(-t + t_d)$, and hence the correlator impulse response is the conjugate of time-reversed version of the received desired signal $\tilde{x}(t)$, that generates the maximum impulse-energy. The SAW correlator behaves like an MF, and operates as a signal compressor resulting in an increase in the output SNR. Considering the input noise $S_{in}(\omega)$ as an Additive White Gaussian Noise (AWGN) and substituting $S_{in}(\omega) = n_{in,0}/2$, which represents two-sided spectral density in Equation 3.5, gives $|y(t_d)|^2 = E_x^2$ and $\overline{|n_{out}(t)|}^2 = n_{in,0}E_x/2$, where E_x is the output signal energy. Based on Equation (3.4), the device output peak instantaneous SNR is defined as in Equation (3.9), where the device noise correlation with the SAW correlator impulse response does not influence the output SNR as shown in the MF derivation.

$$SNR_{peak} = \frac{2E_x}{n_{in,0}} \tag{3.9}$$

To obtain the optimal device response, the mathematical analysis concludes that the time-reversed version of the device impulse response is used as an input excitation signal to the SAW correlator during device measurements.

Equivalent Circuit Model

The impulse response of a single IDT pair is electrically modeled using Mason equivalent circuit as shown in Figure 3.9. To calculate the IDT pair frequency response, conductance, impedance and device IL, three model parameters are defined, which refer to the radiation conductance $G_a(f)$, the acoustic susceptance $B_a(f)$ and the IDT pair total capacitance C_{Total}. The equivalent circuit model equations are based on [46], [51], [52].

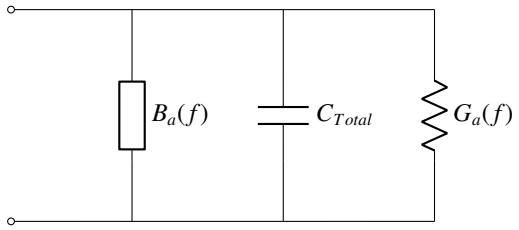


Figure 3.9: *Mason equivalent circuit model of an IDT pair [46], [51].*

The IDT pair impulse transfer function is calculated using the sinc function as expressed in Equation (3.10)

$$|H(f)| = 2k\sqrt{C_s f_0} N_p \frac{sin(X)}{X} e^{\frac{-2j\pi f N_p}{2f_0}} \tag{3.10}$$

Where $X = N_p \pi \frac{(f-f_0)}{f_0}$. f is the frequency and f_0 is the device center frequency, N_p defines the device number of IDT pairs, k is the piezoelectric material coupling coefficient and C_s defines the capacitance for an IDT finger pairs per unit length. If the device input or output port has multiple IDT finger pairs, then the total transfer function is defined as in Equation (3.11).

$$H_{Total}(f) \cong H_1(f).H_2(f)...H_n(f) \tag{3.11}$$

When an RF signal is applied to the IDT pair, the surface wave power is proportional to the radiation conductance $G_a(f)$, which represents the real part of the IDT pair admittance. The radiation conductance is defined in Equation (3.12).

$$G_a(f) = 8k^2 C_s W_a f_0 N_p^2 \left| \frac{sin(X)}{X} \right|^2 \tag{3.12}$$

Where W_a is the IDT aperture, which is defined in Equation (3.13).

$$W_a = \frac{1}{R_{in}} \frac{1}{2 f_0 C_s N_p} \frac{4k^2 N_p}{(4k^2 N_p)^2 + \pi^2} \tag{3.13}$$

Where R_{in} is the IDT pair input resistance. The imaginary part of the IDT pair admittance is called the acoustic susceptance $B_a(f)$, which is expressed in Equation (3.14).

$$B_a(f) = \frac{G_a(f_0) sin(2X) - 2X}{2X^2} \tag{3.14}$$

The combination of the real and imaginary parts is expressed as $Y(f) = G_a + j2\pi f C_{Total} + jB_a$, where the total static capacitance of multiple IDT pairs (such as BPSK Barker-coded output port) is calculated by multiplying the capacitance per unit length with the IDT finger aperture times the IDT finger pairs number $C_{Total} = N_p C_s W_a$, this shows that the output port imaginary impedance component is capacitive, which requires an impedance matching network on the device output as it is shown in Chapter 5. Inverting the total admittance $Y(f)$ gives the IDT pair impedance expression as in Equation (3.15).

$$Z(f) = \frac{1}{G_a + j2\pi f C_{Total} + jB_a} \tag{3.15}$$

The SAW device IL is a function of the frequency as expressed in Equation (3.16), where the device exhibits minimum losses at the center frequency f_0, where R_l is the load resistance.

$$IL(f) = -10 \log \left[\frac{2G_a(f) R_l}{(1 + G_a R_l)^2 + \left[R_l (2\pi f C_{Total} + B_a(f)) \right]^2} \right] \tag{3.16}$$

Finite Element Method (FEM)

In FEM, the SAW device parameters and response are mathematically equivalent to the solution of Partial Differential Equations (PDE) of the piezoelectric substrate. The solution of the PDE gives an accurate model of SAW devices taking into account the effect of device geometry, material type and further parameters that previous two modeling methods either neglect or use a simplified models for them. The boundary conditions method is one of the common methods that the FEM uses to model quantitatively the physical effect of SAW devices, where periodic boundary conditions are fed to the device simulation. The FEM is not considered in details, for more explanations refer to [51], [53]–[55].

3.3 Receiver Sensitivity Analysis

The sensitivity analysis calculates the minimum detectable received power at a certain Bit Error Rate (BER). As shown in the proposed architecture in Figure 2.27, three major subsystems contribute to the total receiver sensitivity. In this section, the effect of the font-end, baseband amplification and the NBC is analyzed, providing the details of each part contribution to the total receiver sensitivity [A5], [56].

3.3.1 RF Front-end

The WuRx RF front-end consists of 13-bits BPSK Barker-coded SAW correlator, followed by an RF envelope detector as shown in Figure 2.27. Given that the SAW correlator output impedance and the RF envelope detector input impedance are conjugately matched, the total RF front-end noise figure NF_{Total} is expressed as in Equation (3.17):

$$NF_{Total} = NF_{SAW} \times NF_{ED} \tag{3.17}$$

The definitions of the front-end noise and the signal power components are given in Figure 3.10. The SAW correlator output noise $n^2_{SAW,out} = n^2_{ED,in}$ is subject to the device IL and has no power compression gain, while Equation (3.18) expresses the SAW output signal power $x^2_{SAW,out} = x^2_{ED,in}$, which is subject to both compression gain and device IL.

$$x^2_{SAW,out} = x^2_{ED,in} = x^2_{SAW,in} \times A_p \tag{3.18}$$

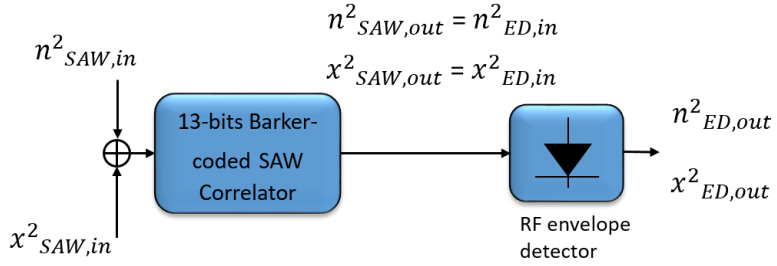


Figure 3.10: *The RF front-end signal and noise power components*

The SAW compression gain A_p equals ideally to 13, which is the Barker code length used in the SAW correlator design, while the amplitude gain equals to $\sqrt{13} = 3.6$. A_p highly depends on the used Piezoelectric material, device modeling and fabrication accuracy. Based on Equation (3.18), the NF_{SAW} is calculated as:

$$\begin{aligned} NF_{SAW} &= \frac{SNR_{SAW,in}}{SNR_{SAW,out}} \\ &= \frac{x^2_{SAW,in}}{n^2_{SAW,in}} \times \frac{n^2_{SAW,in} \times IL}{x^2_{SAW,in} \times A_p} \end{aligned} \tag{3.19}$$

From Equation (3.19), the $NF_{SAW} = IL/A_p$. Based on the design and simulation of the 13-bits BPSK Barker-coded SAW correlator, which is explained in details in Chapter 4, the device has an IL of 11 dB, while providing a power compression gain $A_p = 4$ [8], [A1]. In [56], the output SNR of an envelope detector using a squaring device was analyzed. Applying the same mathematical analysis to the receiver RF front-end, the SNR_{out} is expressed in Equation (3.20).

$$SNR_{ED,out} = \frac{x_{ED,in}^2}{8x_{ED,in}^2 \times n_{ED,in}^2 + 4n_{ED,in}^4} \frac{BW_{RF}}{BW_{BB}} \tag{3.20}$$

where BW_{RF} and BW_{BB} refer to the RF bandwidth and baseband bandwidth, respectively. Substituting the noise power components from Equation (3.18) into Equation (3.20), and solving the quadratic equation for the input signal power $x_{ED,in}^2$, the receiver front-end sensitivity is defined in Equation (3.21), where $P_{sens,FE}$ is the minimum detectable input signal power by the receiver and SNR_{min} is the minimum SNR to achieve a specified BER.

$$P_{sens,FE} = \frac{4KT \times SNR_{min}\, NF_{Total}\, BW_{BB}}{A_p} + \frac{2KT \times NF_{Total} \sqrt{4BW_{BB}^2 SNR_{min}^2 + BW_{RF} BW_{BB} SNR_{min}}}{A_p} \tag{3.21}$$

Table 3.7 shows the receiver front-end sensitivity with the parameters substituted in Equation (3.21). The poor sensitivity of the RF front-end is caused by the elimination of the RF LNA, which has smaller NF compared to the RF envelope detector, and because of the large baseband noise bandwidth.

Table 3.7: *Front-end sensitivity*

Parameter	Value
BW_{RF}	80 MHz
BW_{BB}	33 MHz
NF_{Total}	45.5 dB
SNR_{min}	12.5 dB
BER	1×10^{-3}
A_p	4
$P_{sens,FE}$	−38 dBm

3.3.2 Baseband Amplification

This section explains the effect of the baseband amplification on the total receiver sensitivity. As shown in the proposed architecture in Figure 2.27, the RF envelope detector is

followed by a baseband amplifier. The Baseband amplification is required when the front-end gain is insufficient for further signal processing. The impact of the baseband amplification noise on the overall receiver sensitivity should be analyzed. The noise of the baseband amplifier consists of Flicker and thermal noise. Figure 4.22 in Chapter 4, shows the simulated baseband amplifier Power Spectral Density (PSD) of the input-referred noise. At frequencies below the $1/f$ noise corner f_{cor}, the noise PSD is dominated by $1/f$ noise. After that, the thermal noise floor PSD_0 of the baseband amplifier is dominating. For thee analytical noise analysis, the BW_{BB} which is the total baseband noise bandwidth is defined in Equation (3.22), where N equals the ratio between f_{max} and f_{min}. The value of f_{min} equals to 4.2 MHz, which is the SAW pulses rate of 238 ns as shown in Figure 5.7.

$$BW_{BB} = f_{max} - f_{min} = (N-1) \times f_{min} \tag{3.22}$$

The thermal baseband noise is defined in Equation (3.23), where PSD_0 is the input-referred noise floor.

$$\overline{v_{n,th}^2} = PSD_0 \times BW_{BB} \tag{3.23}$$

The total $1/f$ noise is expressed in Equation (3.24).

$$\overline{v_{n,1/f}^2} = PSD_0 \times f_{cor} \times \ln N \tag{3.24}$$

Adding Equations (3.23) and (3.24) together, the total baseband noise is defined in Equation (3.25).

$$\overline{v_{n,total}^2} = PSD_0 \times (BW_{BB} + f_{cor} \times \ln N) \tag{3.25}$$

Based on [56], the baseband power sensitivity is defined in Equation (3.26). Where $A_{v,ED}$ is the RF envelope detector conversion factor. Table 3.8 shows the receiver baseband sensitivity with the parameters used in the calculation. From Equation (3.26), the receiver baseband sensitivity can be further improved by maintaining smaller baseband bandwidth and larger front-end amplification as well as minimizing the input-referred noise.

$$P_{sens,BB} = \frac{20 \times \sqrt{SNR_{min} PSD_0 \times (BW_{BB} + f_{cor} \ln N)}}{A_{v,ED} \times A_p} \tag{3.26}$$

3.3.3 Narrowband Correlator

The node ID is encoded in Pulse Position Modulation (PPM) scheme, where the time distance between two successive amplified envelope detected pulses represents logic zero or one. The idea of the narrowband detector is to reduce the baseband bandwidth using multiple envelope detected pulses instead of one to implement the PPM scheme. The BW_{BB} is taken to be equal to 33 MHz, which depends on the bit time of the used Barker code. From the output of the narrowband correlator, the same PPM information is extracted from multiple detected and amplified signals. As an example of the sensitivity improvement working principle, when the receiver noise bandwidth is reduced from 33 MHz

Table 3.8: *Baseband sensitivity*

Parameter	Value
BW_{BB}	33 MHz
SNR_{min}	12.5 dB
BER	1×10^{-3}
PSD_0	15×10^{-18} V^2/Hz
f_{cor}	5 kHz
N	9
A_p	4
$A_{v,ED}$	4
$P_{sens,BB}$	−39 dBm

(which is equivalent to the enveloped signal bandwidth) to 1 MHz, the contribution to the total receiver sensitivity by means of the narrowband receiver is calculated as below:

$$10 \log_{10}(1\,\text{MHz}/33\,\text{MHz}) = -15.1\,\text{dB}$$

Reducing the noise bandwidth improves the total sensitivity by factor of 15.1 dB. Adding this improvement to the front-end sensitivity, since it has lower value compared to the baseband amplification sensitivity, yields to a total sensitivity of −53.1 dBm. Reducing the baseband bandwidth to 1 MHz results in further improvement of the receiver sensitivity, however, the communication data-rate is further reduced.

3.4 Link Budget and Range

The link budget analysis calculates the transmitted signal power loss through the communication medium, reaching to the receiver. Figure 3.11 shows the communication link between the transmitter and the receiver with the analytical quantities used in the link budget calculation.

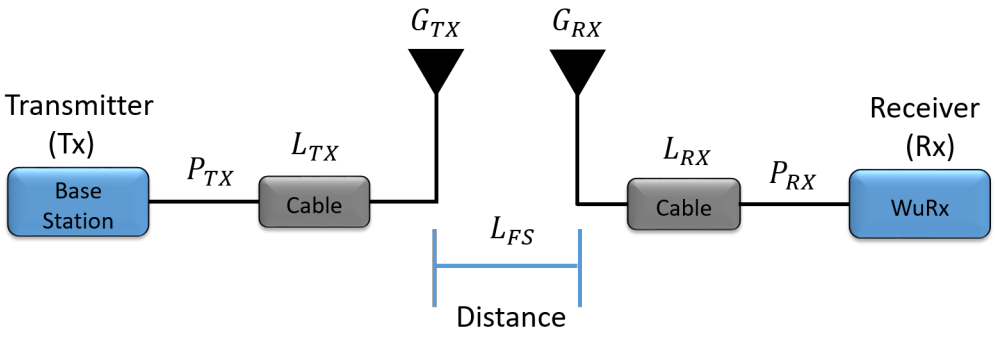


Figure 3.11: *Communication link*

Equation (3.27) calculates the received power P_{RX}, which is defined by adding up the average transmitted power P_{TX}, the transmitter and the receiver antenna gain, which are de-

fined as G_{TX}, G_{RX} respectively and the free path power losses expressed as $20\log(\frac{\lambda}{4\pi Distance})$ [11].

$$P_{Rx}|_{dbm} = P_{Tx}|_{dBm} + G_{Tx}|_{dBi} + G_{Rx}|_{dBi} + 20\log(\frac{\lambda}{4\pi Distance}) \tag{3.27}$$

From Section 3.3, the total receiver sensitivity is −53.1 dBm, which corresponds to 70 m direct-sight communication of distance based on the link budget calculation shown in Table 3.9. The calculation assumes 1 dB of transmitter and receiver cable losses L_{Tx} and L_{Rx}, furthermore, the antenna gains G_{Rx} and G_{Rx} are assumed to be 3 dBi. The average transmitted power at 2.44 GHz is 20 dBm [47].

Table 3.9: *Link budget calculation parameters*

Parameter	**Value**
P_{Tx}	20 dBm
G_{Tx}	3 dBi
G_{Rx}	3 dBi
L_{Tx}	1 dB
L_{Rx}	1 dB
λ	0.125 m
Distance	70 m

3.5 WuRx Chip Design Target

The target is to design an always-on WuRx that operates for several years without battery replacement. Obtaining less than 100 µW average power dissipation enables the WuRx to operate for almost three years, when powering it up with 1.2 V and 2000 mAh battery. According to the sensitivity analysis and the link budget calculations carried out in this chapter, the receiver communication range reaches 70 m, which is considered sufficient in wide range of WSN applications. The data-rate is also another design target, which is desired to be more than 100 kbps. Table 3.10 summarises the WuRx IC design target.

Table 3.10: *WuRx IC design target*

Design parameter	**Expected value**
Power dissipation	$\leqslant$ 100 µW
Sensitivity	−53.1 dBm
Communication range	70 m
Data-rate	$\geqslant$ 100 kbps
Co-channel interference robustness	Yes
Chip area	$\leqslant$ 1 mm^2

3.6 Summary

This chapter starts with defining the basic design considerations and challenges in WSN. Reducing power dissipation in WSN and providing robustness against co-channel and

noise improves the WSN nodes operating lifetime and false positive communication. The proposed WuRx IC architecture is based on direct-detection to achieves low-power dissipation levels, however, it has poor sensitivity as shown in the receiver sensitivity analysis. The analysis shows that reducing the baseband bandwidth contributes to the total receiver sensitivity. The analysis proposes the use of a NBC to reduce the baseband bandwidth versus communication data-rate.

In this chapter, the use of the SAW correlator to provide a passive co-channel interference robustness is proposed. For that, a 13-bits BPSK Barker-coded SAW works at 2.44 GHz is selected for design and fabrication. The choice of the SAW correlator working scheme is based on a feasibility study from [8], [9]. Several modeling methods of the SAW correlator is discussed. From the mathematical model, it concludes that in order to achieve the optimal correlation, the SAW correlator is designed in a way that the impulse response is the time-reversed version on the input excitation signal. The equivalent model of the SAW correlator shows that the output impedance of the SAW correlator is capacitive, and needs an external serial inductor in order to be matched to 50 Ω at the working frequency.

4 Components Level Design and Simulation

This chapter presents in detail the design and simulation of the WuRx. Based on the block diagram of the WuRx shown in Figure 2.27, the chapter starts with the design and simulation of the 13-bits 2.44 GHz BPSK Barker-coded SAW correlator, more details about the SAW design found in [8], [A1]. Subsequently a detailed design and simulation of the WuRx IC components implemented in CMOS TSMC65nm technology are presented.

4.1 SAW Correlator Design and Simulation

Based on the system analysis explained in Chapter 3, a 13-bits 2.44 GHz BPSK Barker-coded SAW correlator is selected for design and fabrication. The selection of the device signal modulation, frequency and other material parameters presents a trade-off between the design requirements and the fabrication feasibility. The company frecnsys designed and fabricated the device as a subcontractor to the Paderborn university. To explain the BPSK Barker-coded SAW correlator design concept of the device, an example of 4-bits device is shown in Figure 4.1 [A1].

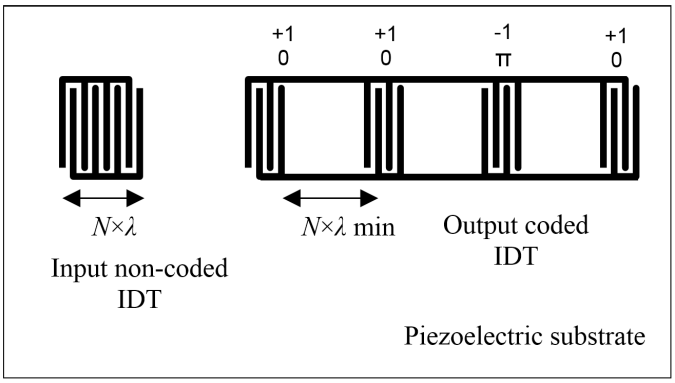
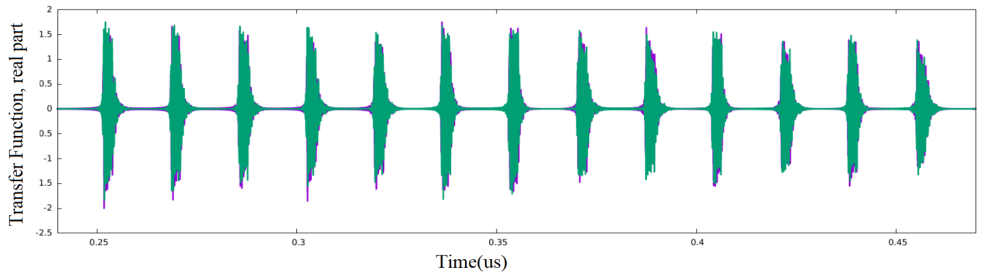


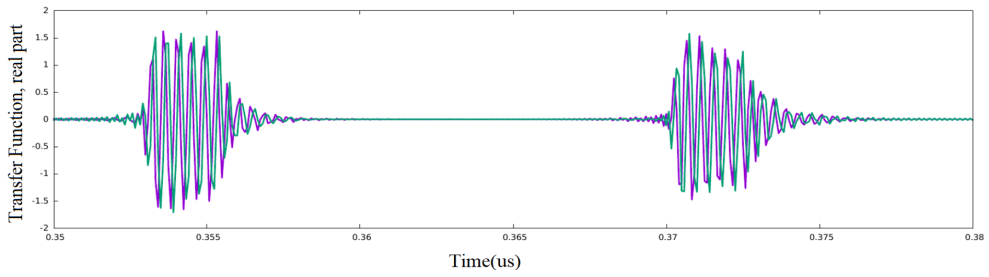
Figure 4.1: *General structure of a 4-bits BPSK Barker-coded SAW correlator [A1]*

The device is composed of three main parts, the input port, which is called the non-coded IDT port, a Lithium Niobate $LiNbO_3$ substrate, which is selected for design and fabrication according to the system analysis carried out in Chapter 3, and the output BPSK Barker-coded port. The device operating principle is based on converting the input RF excitation signal into an acoustic wave via the input port. The acoustic wave is then convolved at the acoustic wave speed of the Lithium Niobate $LiNbO_3$ substrate, with the phase modulated IDTs on the output port, where it is converted back into electrical signal. Figure 4.1 shows that the BPSK modulation scheme of the SAW device is obtained by alternating the IDT fingers phase. If every code consists of multiple IDTs pairs, then changing the phase is achieved by rotating the complete set of IDTs by 180°. Each bit of the device is composed of multiple IDTs which forms a set. The output port IDT sets are separated from each other by an integer number N of acoustic wavelength. In BPSK SAW devices, the separation equals to (or larger than) the length of the excitation IDT. The designed SAW correlator is a 13-bits Barker-coded device, with BPSK

Barker code sequence (+1, +1, +1, +1, +1, -1, -1, +1, +1, -1, +1, -1, +1). The selected device is compatible with standard SAW manufacturing capabilities, with one type of wavelength in the whole device and a finger-width of 400 nm using Rayleigh waves on $LiNbO_3$ (YX)/128° [8], [9], [A1]. The device electrical response is based on combining the non-coded input port and a Barker-coded output port using the mixed matrix model, which defines the device center frequency, where the device IL is minimum. The device wavelength is set to 1.6 µm considering Lithium Niobate $LiNbO_3$ substrate phase velocity of 3970 m/s and crystal orientation of (YX)/128°, which is particularly suitable for the design and fabrication as it exhibits a limited reflection coefficient of the waves on the IDT electrodes. The IDT electrode height is 80 nm , which is suitable for the device manufacturing electrode integrity. The metalization ratio, which is defined as the ratio between the IDT width and the pitch is set to 0.5 and the relative IDT electrode height of h/λ is 5 %. The reflection coefficient is set to 2 %. Choosing the IDT height 50 nm yields smaller reflection value, but higher resistive losses. Optimally, the device operation requires to match the input and the output port to 50 Ω. As a consequence, the optimal finger pair number of the non-coded IDT is taken to be between 16 and 20, where each bit of the coded IDT is composed of 6 IDT finger pairs. As demonstrated in Chapter 3, the best input excitation sequence is the time-reversed version of the device impulse response, which is obtained by the inverse Fourier transform of the simulated device as shown in Figure 4.2.



(a)



(b)

Figure 4.2: *Time-domain signal provided by a 13-bits 2.44 GHz Barker code with 6 wavelengths per bit (a) Total signal sequence showing the 13-bits and the time-delay between each bit corresponding to 36 wavelengths [8], [A1] (b) Zoom on the 7_{th} and 8_{th} bits, showing the phase change between the two bits [8], [A1]*

The transformation is taken on a wide band from 0.1 GHz to 6 GHz to provide enough points for the impulse response, especially when the IDT phase changes from +1 to -

1. Each coded IDT bit is separated by 36 wavelength, which makes the total length 57.6 µm. With this configuration, the device coded port length is less than 2mm [8], [A1]. Depending on the above mathematical analysis, but with increasing the output port coded IDT pairs to 18. The device transfer function is shown in Figure 4.3, where the device has the minimum IL at 2.44 GHz.

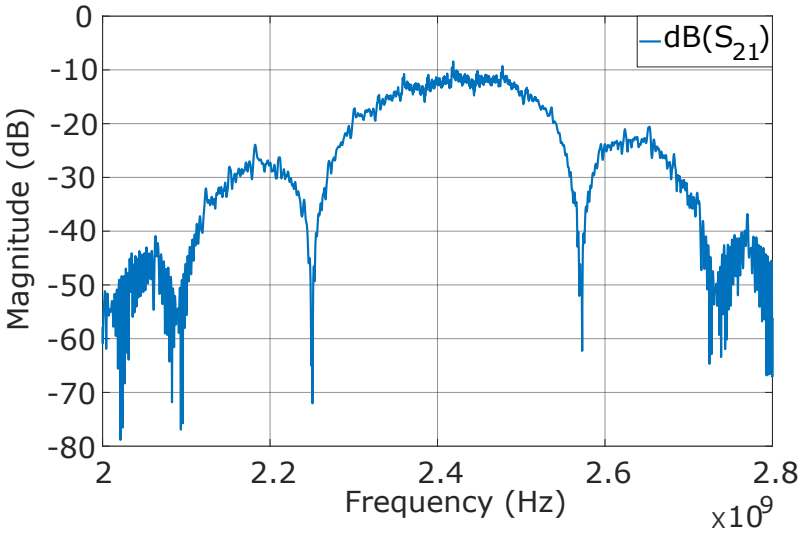


Figure 4.3: *Simulated 2.44 GHz BPSK Barker-coded SAW correlator transfer function [8]*

The device reflections coefficients S_{11} and S_{22} are shown in Figure 4.4. The input port of the device is matched to 50 Ω at 2.44 GHz, while the output port is not, and needs an external series inductor matching network, since the output port imaginary part impedance is capacitive.

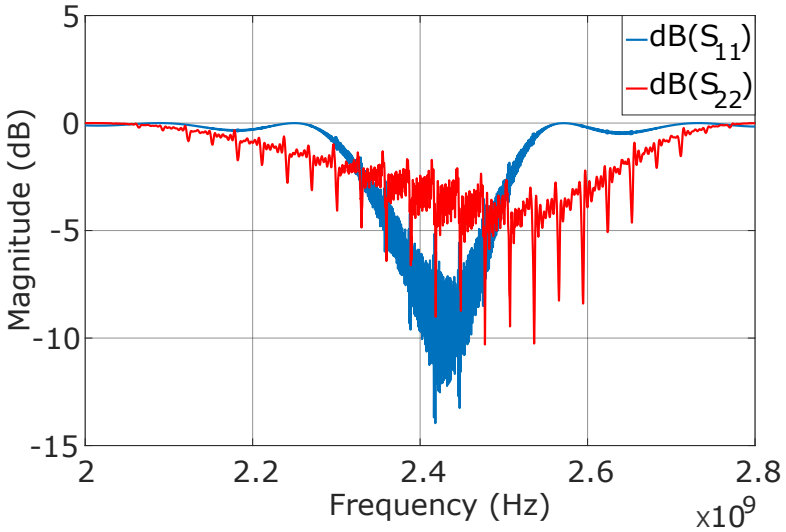


Figure 4.4: *Simulated 13-bits 2.44 GHz BPSK Barker-coded SAW correlator input and output reflections coefficients [8]*

Figure 4.5 shows the SAW correlator relative impulse response for a 13-bits SAW correlator obtained by inverse Fourier transform.

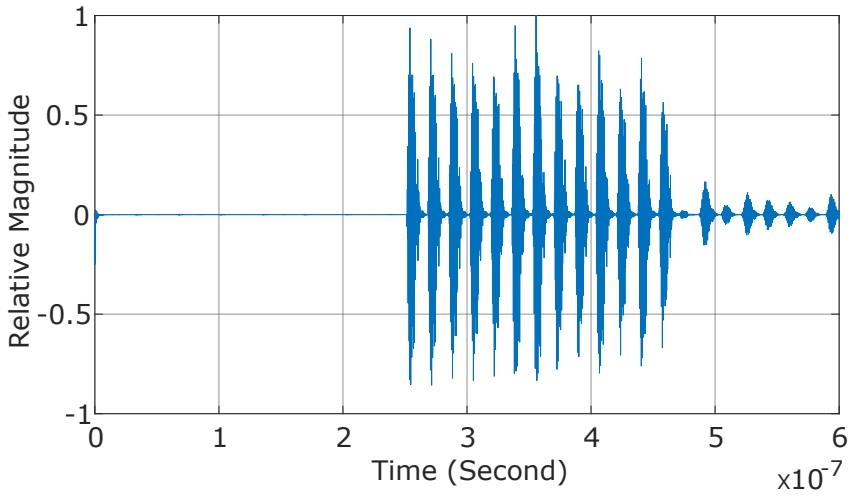


Figure 4.5: *Simulated 13-bits 2.44 GHz BPSK Barker-coded SAW correlator impulse response [8]*

To obtain the best correlation and device response, and according to [8], Figure 4.6 shows the input excitation signal synthesis. Each bit is composed of 24 sine waves at 2.44 GHz, with additional delay. The bit wave time τ is equivalent to 16.835 ns, which makes the wave time of the 13-bits 2.44 GHz time-reversed Barker-coded signal equals to 218.855 ns.

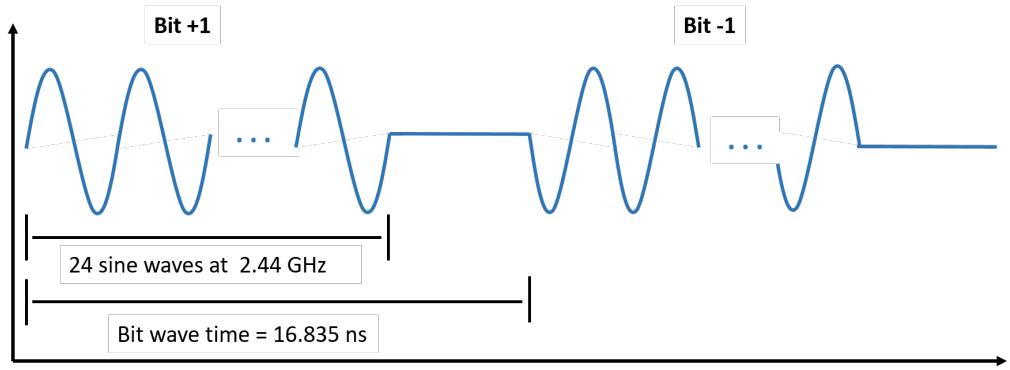


Figure 4.6: *Input signal synthesis for the optimal input signal/impulse response correlation [8]*

Figure 4.7 shows the relative time-domain output for single input/output 13-bits 2.44 GHz SAW correlator as a result of 13-bits 2.44 GHz BPSK time-reversed Barker-coded sine wave signal. The output represents a sharp RF pulse with width equals to 2τ, where τ represents a single bit wave time. The simulated amplitude gain is $A_v = 0.45$, which corresponds to 5 to 6 dB of compression gain. The deviation between the theoretical compression gain and the simulated device comes from multiple factors, such as the design capabilities, the material used and the electro-mechanical coupling. For more detailed information about the SAW correlator design and simulation, refer to [8], [9], [A1].

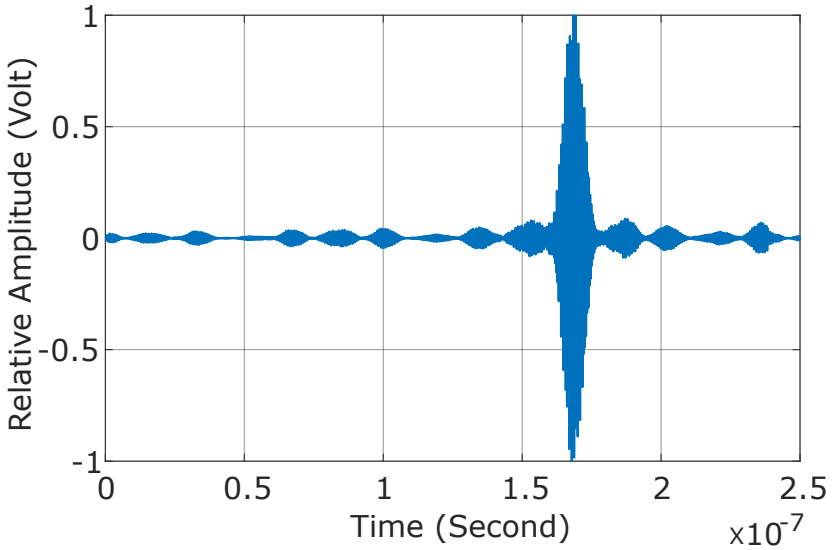


Figure 4.7: *Relative time-domain simulated output for single input/output SAW correlator excited with periodic 13-bits 2.44 GHz BPSK Barker-coded signal [8]*

4.2 RF Envelope Detector

The SAW correlator is followed by a self-biased active RF envelope detector that down-converts the RF output signal of the SAW correlator to a baseband signal. The SAW correlator output and the RF envelope detector input impedance are conjugated-matched to provide the maximum power delivery from the SAW correlator to the RF envelope detector. The schematic of the self-biased active RF envelope detector is shown in Figure 4.8. The RF detector is a self-biased Common Source (CS) envelope detector, with an impeded input matching network. The RF envelope detector core is composed of differential input transistors M_{n1} and M_{n2} with a large self-biasing resistor R_f that provides an isolation between the input and the output of the RF envelope detector. The input transistors are RF NMOS transistors with low threshold voltage to fit the low-power design requirements. The R_f is realized by a pseudo resistor, providing large resistance value and small area. The source terminal of the transistors M_{n1} and M_{n2} is connected to a center-tapped low-quality factor inductor L_s to provide the real-part for the input impedance matching, while the gate inductors (L_{G1}, L_{G2}) of M_{n1} and M_{n2} are external inductors that remove the imaginary part of the input impedance, providing a narrowband matching and suppressing out-of-band input signals. The two capacitors C_{ex1} and C_{ex2} are RF Metal-Insulator-Metal Capacitor (MIMCAP), that are added in parallel to the input transistor C_{gs} providing additional parameter in the input impedance matching. The DC block capacitors C_{ac1} and C_{ac2} must be large enough compared to $C_t = C_{ex} + C_{gs}$ to provide the maximum signal swing at the differential input transistors. The output capacitor C_{out} operates as a low-pass filter and sustains the output voltage signal. The envelope RF detector is biased with a low-current, keeping the transistor biasing in the sub-threshold region. When there is no input signal at the input transistor, V_{gs} equals to the transistor threshold voltage. However, when there is an input RF signal, the RF detector drain current increases exponentially while the DC biasing current I_{bias} is maintained the same. This working principle results in a discharge current of the low-pass output capacitor, and the output voltage V_{out} drops

until I_{bias} is equal to $I_{n1} + I_{n2}$. As a result, an envelope shape of the input RF signal with 180° signal phase shift between the input and the output is achieved.

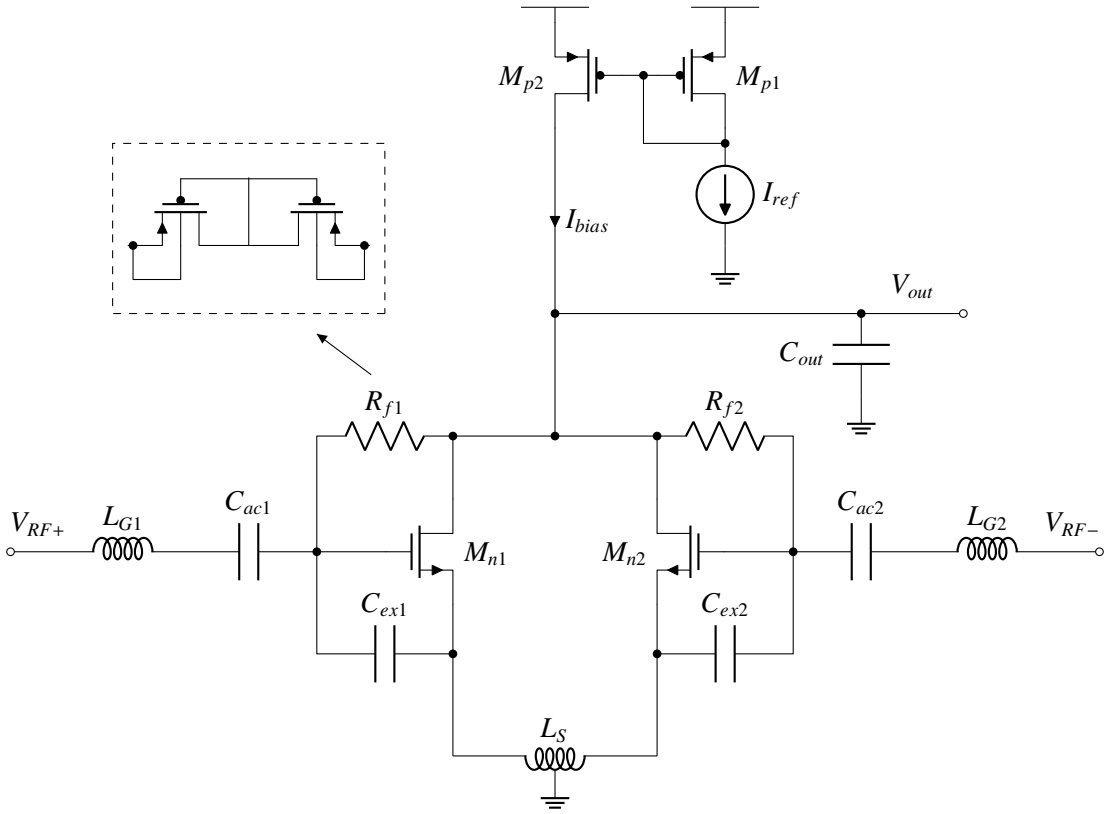


Figure 4.8: *Self-biased active RF envelope detector [57]*

The detector output voltage is expressed in Equation (4.1) [17], [57], [58]:

$$V_{out} = \frac{-I_{bias} R_{out} Q^2 A_{in}^2}{4(nV_T)^2} \tag{4.1}$$

where R_{out} is the RF envelope detector output resistance. A_{in} is the peak amplitude of the RF input signal, and Q is the matching network quality factor, which equals to $Q = 1/(\omega_0 R_s C_t)$ where R_s is the RF signal source output impedance. The sub-threshold slope factor equals to n, and V_T is the thermal voltage. From the above equation, the envelope detector output peak increases with the DC biasing current, however, this increases the static power dissipation. In addition, maintaining a narrowband impedance matching provides a passive amplitude boost to the input RF signal, which increases the detector output peak as well. The RF envelope detector voltage normalized conversion gain is expressed in Equation (4.2) [58]:

$$G_{v,con} = \frac{\partial V_{out}}{\partial A_{in}^2} = \frac{-I_{bias} R_{out} Q^2}{4(nV_T)^2} \tag{4.2}$$

The RF envelope detector layout is shown in Figure 4.9. The circuit core is mainly composed of the input RF transistors. The large source low-quality factor inductor provides the real part of the input impedance. However, it occupies most of the RF detector layout

size. The power ring is composed of a series of capacitors connected between supply voltage and ground to provide an AC ground path.

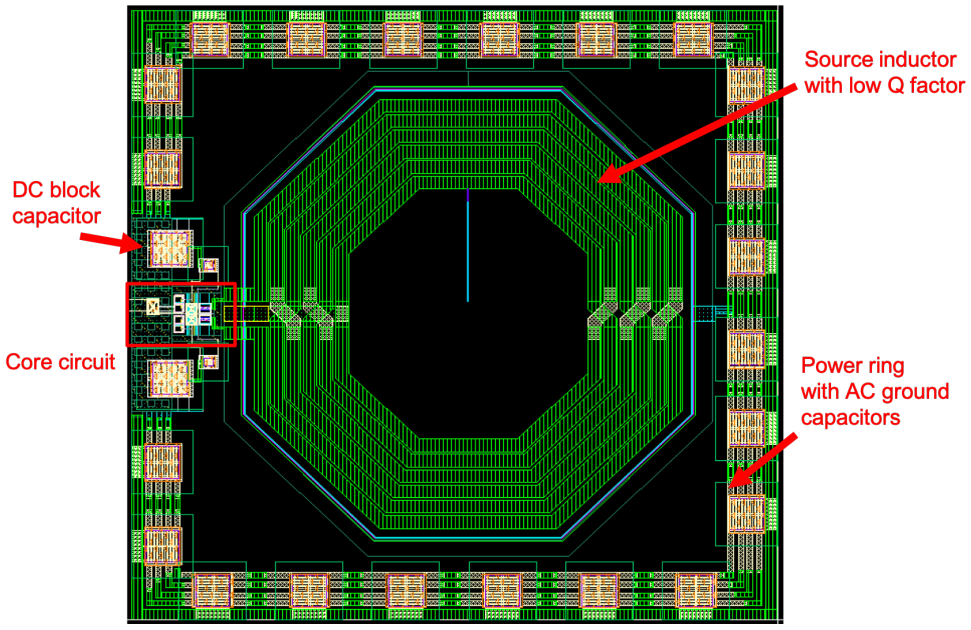


Figure 4.9: *RF envelope detector layout*

The pre- and post-layout time-domain simulation of the RF envelope detector is shown in Figure 4.10. For a 5 mV differential output of the SAW correlator, a 15 mV peak baseband signal is generated. Small deviation in the peak time width between pre- and post-layout is due to additional parasitic capacitance in the layout.

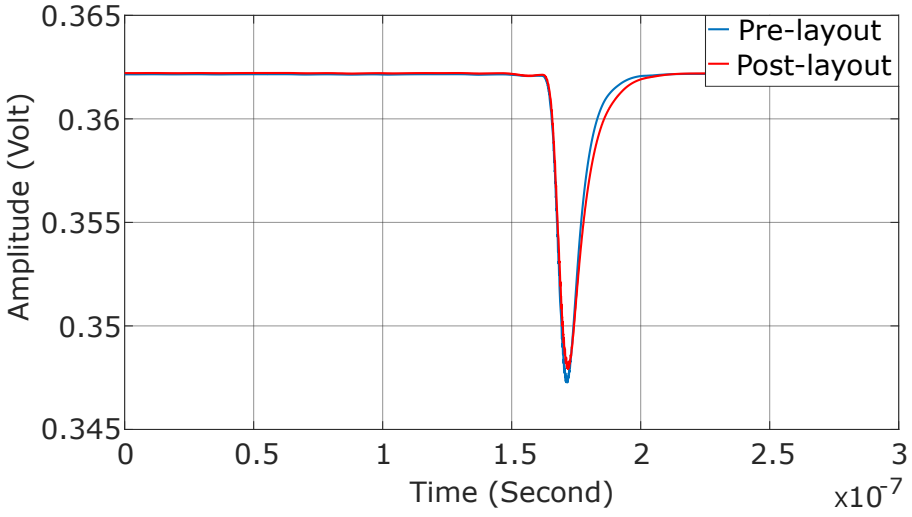


Figure 4.10: *Pre- and post-layout simulation of the RF envelope detector transient output for 5 mV differential input signal*

Figure 4.11 shows the pre- and post-layout simulation of different output detected peak values with respect to several differential input signals. The input/output conversion becomes larger with respect to higher input signal swing, where the input transistors no longer operate in sub-threshold region.

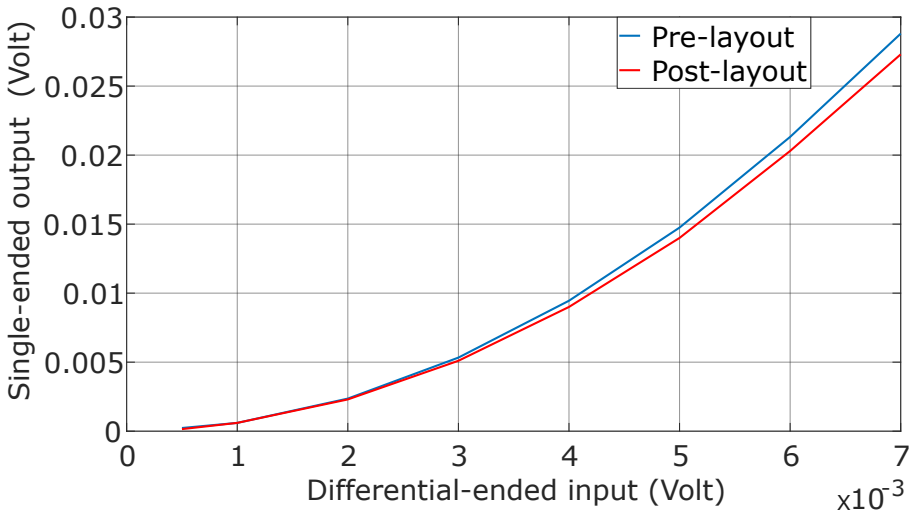


Figure 4.11: *Pre- and post-layout simulation of the RF envelope detector input vs. output*

Input Impedance

Figure 4.12 shows the schematic of the small signal half equivalent circuit for the RF envelope detector. The impedance analysis of the RF envelope detector is based on [17], [57], [58]. The RF envelope detector with the resistive feedback input impedance is expressed in Equation (4.3):

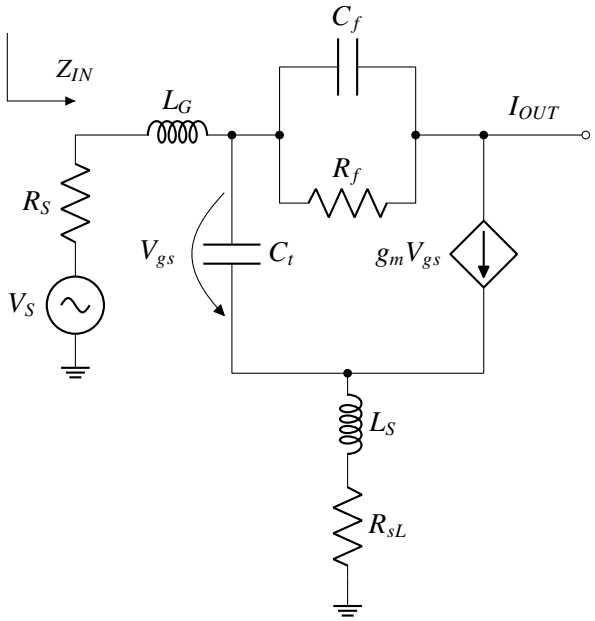


Figure 4.12: *RF envelope detector small signal half equivalent circuit [57]*

$$Z_{IN} \approx sL_g + \left(R_f \parallel \frac{1}{sC_f}\right) \parallel \left[\frac{g_m L_s}{C_t} + R_{sL} + sL_s + \frac{1}{sC_t}\right] \tag{4.3}$$

The input impedance is equivalent to RLC circuit in parallel with the feedback resistor R_f.

The whole term is then added in series with the gate inductor L_G. The feedback resistance is sufficiently large, so Equation (4.3) is simplified as in Equation (4.4):

$$Z_{IN} \approx \left[\frac{g_m L_s}{C_t} + R_{sL}\right] + \left[sL_g + sL_s + \frac{1}{sC_t}\right] \tag{4.4}$$

The source inductor L_S exhibits a small quality factor, and hence its series resistance is taken into consideration. The inductor quality factor Q equals to $Q = 1/(\omega_0 R_s C_t)$, at the resonance frequency ω_0, which is expressed in Equation (4.5),

$$\omega_0 = \frac{1}{\sqrt{(C_{gs} + C_{ex})(L_g + L_s)}} \tag{4.5}$$

From the above equation, the larger the C_{ex}, the smaller the source inductor L_s. However, the quality factor Q is reduced, causing the RF envelope detector conversion gain to decrease as well. Figure 4.13 shows the pre- and post-layout simulation of the RF envelope detector input reflection parameter S_{11}. The imaginary part of the input impedance is removed by an off-chip inductor. It is shown that the pre- and post- layout simulated S_{11} are matched at 2.44 GHz. Due to layout parasitics, the post-layout simulated S_{11} has a frequency shift, but still matched at 2.44 GHz.

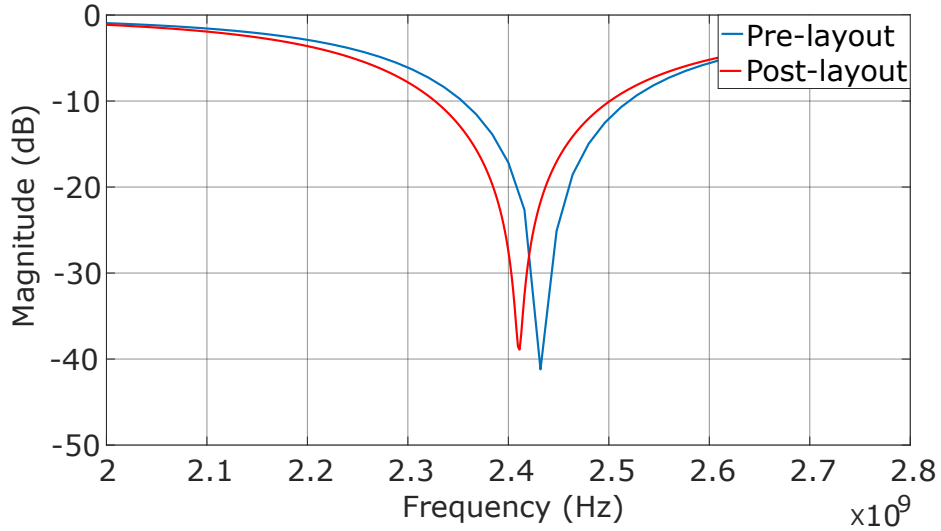


Figure 4.13: *Pre- and post-layout simulation of the RF envelope detector input return loss*

The input matching network of the RF envelope detector provides a passive gain for the RF input signal, which is equivalent to Q^2. Figure 4.14 shows the pre-layout output signal of the SAW correlator (input signal of the RF envelope detector) with and without the passive voltage boost. The boosted signal shape is not changed, however, with the narrowband matching, it is 6 times larger.

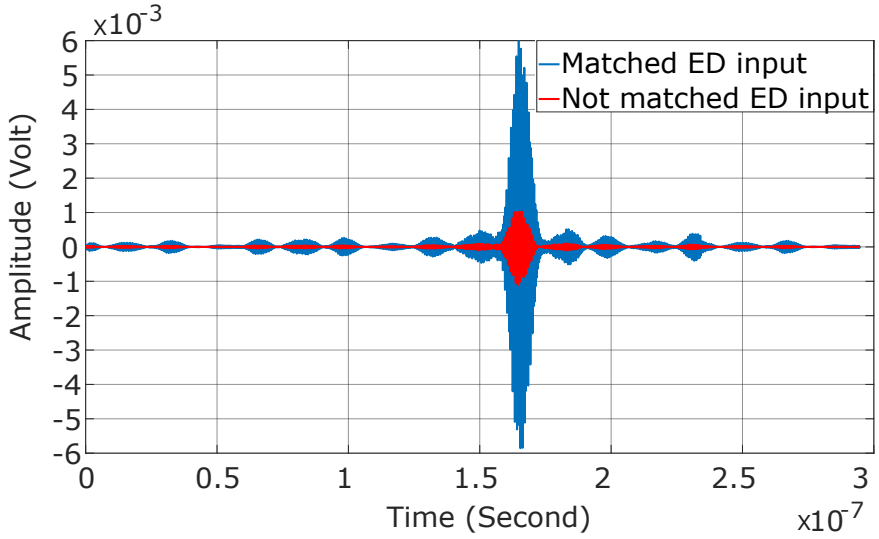


Figure 4.14: *Simulated SAW output w/ and w/o RF envelope detector input impedance matching*

Noise Figure

Figure 4.15 shows the simplified half-circuit RF envelope detector noise model. At baseband frequency, the external gate inductor L_G and the source inductor L_S are considered as a short circuit, while $C_t = C_{ex} + C_{gs}$ is considered as an open circuit. The noise analysis of the RF envelope detector is based on [17], [57], [58].

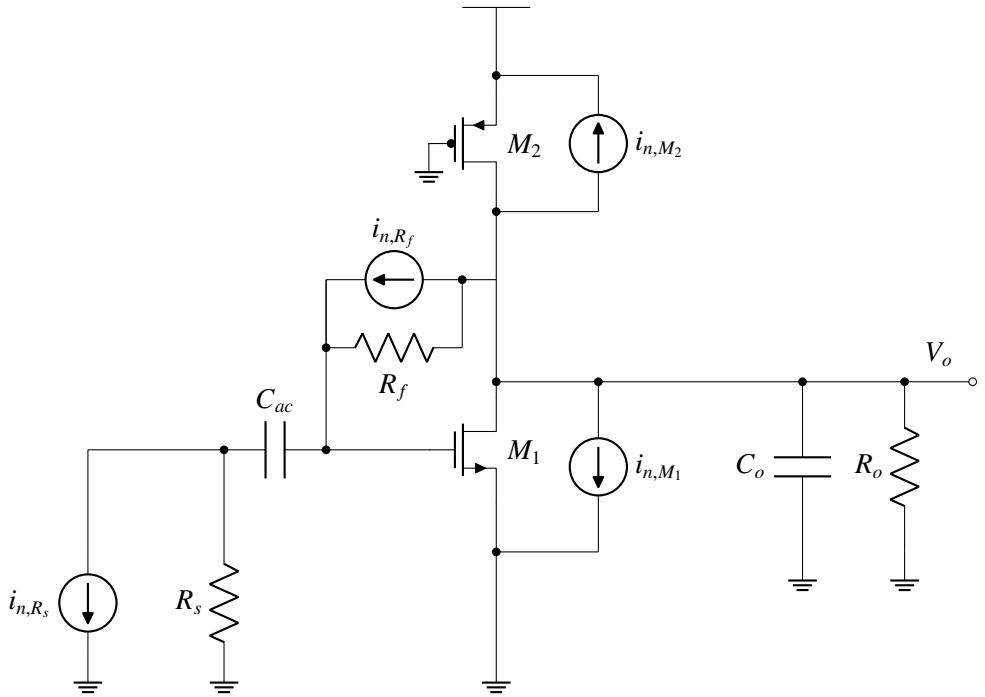


Figure 4.15: *Simplified RF envelope detector noise model [57]*

The thermal noise from the source and the feedback resistors is equivalent to $\overline{I^2_{n,R_s}} = 4kT/R_s$ and $\overline{I^2_{n,R_f}} = 4kT/R_f$ respectively, where K is Boltzman constant. The thermal and

flicker noise sources of the transistors M_1 and M_2 are expressed in Equation (4.6).

$$\begin{aligned}\overline{I_{n,M_1}^2} &= 4kT\gamma g_{m1} + \frac{K_{1/f} g_{m1}^2}{f} \\ \overline{I_{n,M_2}^2} &= 4kT\gamma g_{m2} + \frac{K_{1/f} g_{m2}^2}{f}\end{aligned} \tag{4.6}$$

Where the factor γ is a process factor and ranges from 0.7 to 1. The total noise source of the two transistor is defined as $\overline{I_n^2} = \overline{I_{n,M_1}^2} + \overline{I_{n,M_2}^2}$. Given that in baseband frequency, $R_f \gg R_s$ and $R_s \ll 1/sC_{ac}$, the noise transfer function is expressed in Equation (4.7).

$$H_M \approx \left|\frac{V_o}{I_n}\right| = Z_L \parallel (R_f + \frac{1}{sC_{ac}}) \parallel \frac{R_f}{g_m\left[R_f \parallel \frac{1}{sC_{ac}}\right]} = Z_L \parallel \frac{1}{g_m}\frac{(1 + sC_{ac}R_f)}{(1 + \frac{sC_{ac}}{g_m})} \tag{4.7}$$

The noise transfer function of the R_f to the output voltage V_o is expressed in Equation (4.8), and with similar assumption as above , the term is further simplified to Equation (4.9).

$$H_{R_f} = R_f \parallel Z_L \frac{R_f(\frac{1}{g_m} + R_s + \frac{1}{sC_{ac}})}{(\frac{1}{g_m})(R_f + R_s + \frac{1}{sC_{ac}})} \tag{4.8}$$

$$H_{R_f} \approx R_f \parallel Z_L \frac{g_m R_f(1 + \frac{sC_{ac}}{g_m})}{(1 + sC_{ac}R_f)} \tag{4.9}$$

The total noise of the transistors M_1, M_2 and the feedback resistor R_f is expressed in Equation (4.10).

$$N_{Total} = (\overline{I_{n,M_1}^2} + \overline{I_{n,M_2}^2}).H_M^2 + I_{n,R_f}^2.H_{R_f}^2 \tag{4.10}$$

Figure 4.16 shows the pre- and post-layout output noise Power Spectral Density (PSD). The total RF envelope detector output noise N_{Total} is calculated by integrating the output PSD over the baseband bandwidth.

The definition of the RF envelope detector NF uses Friis' formula as expressed in Equation (4.11).

$$NF_{V_{in}} = 1 + \frac{N_{Total}}{N_s G_{v,con}^2 V_{in}^2} \tag{4.11}$$

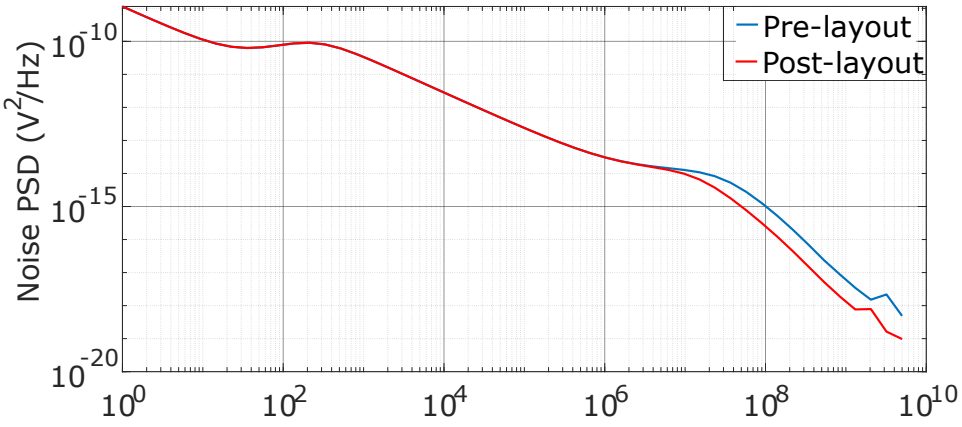


Figure 4.16: *Pre- and post-layout simulation of the RF envelope detector output noise PSD*

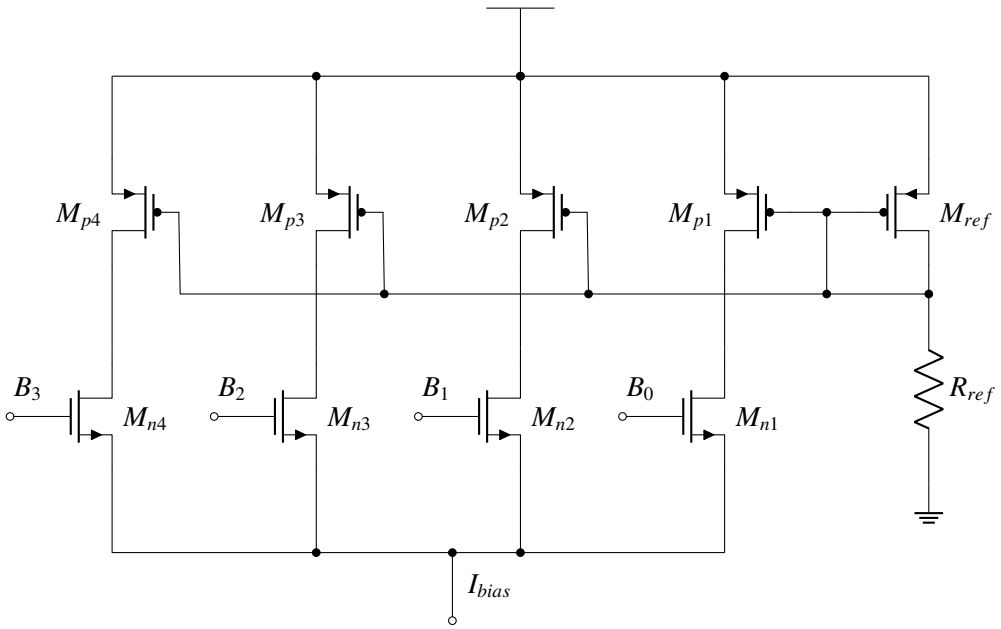


Figure 4.17: *4-bits configurable current mirror*

DC Biasing

Figure 4.17 shows the schematic of 4-bits configurable current mirror. The 4-bits configuration provides freedom to bias the RF envelope detector in different operating regions and not only the sub-threshold region. Additionally, the channel width of the current mirror output transistors M_{p1} to M_{p4} is increasing incrementally, in order to overcome any process or temperature variation.

Table 4.1 shows different biasing configuration, with respect to the biasing current and the operating region. The RF envelope detector input transistor threshold voltage equals to 357 mV.

Table 4.1: *4-bits configurable DC biasing points*

B_0	B_1	B_2	B_3	I_{ref} (µA)		V_{gs} (mV)		Region
				Pre-layout	Post-layout	Pre-layout	Post-layout	
1	0	0	0	7.98	7.98	334.8	334.8	Sub-threshold
0	1	0	0	10.14	10.12	346.6	346.5	Sub-threshold
0	0	1	0	12.30	12.27	356.2	356.0	Sub-threshold
0	0	0	1	14.40	14.35	364.5	365.3	Saturation

4.3 Baseband Amplifier

The detected baseband signal is further amplified by a baseband amplifier with cascaded stages of differential amplifier cells with a total gain of 40 dB, and a 3 dB bandwidth of 100 MHz. From Figure 4.18, the baseband amplifier consists of a split-source and classical stages of differential amplifiers. The split-source differential amplifier is used so that the DC and low-frequency components are removed without affecting the desired amplification bandwidth [18]. The schematic of the used amplifier stages is shown in Figure 4.19.

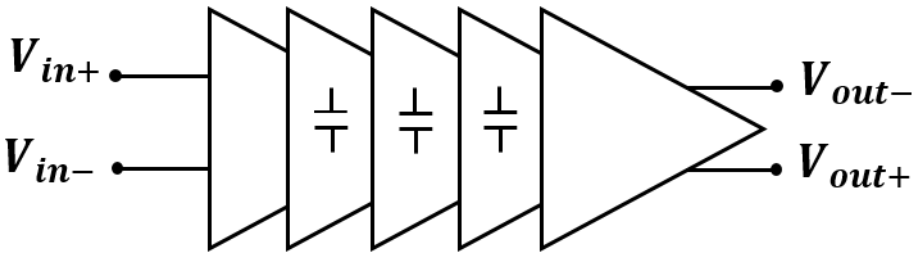


Figure 4.18: *Baseband amplifier block diagram*

Figure 4.20 shows the layout of the baseband amplifier. According to the amplifier transfer function, larger capacitors are used to attenuate the low-frequency components.

The simulated pre- and post-layout baseband amplifier transfer function is shown in Figure 4.21, where the low-frequency inputs signals are attenuated, while the input signal between 1 MHz and 100 MHz are subject to 40 dB of amplification gain.

The pre- and post-layout simulated baseband amplifier input-referred noise PSD is shown in Figure 4.22, where thermal noise dominates for frequencies higher than 100 kHz.

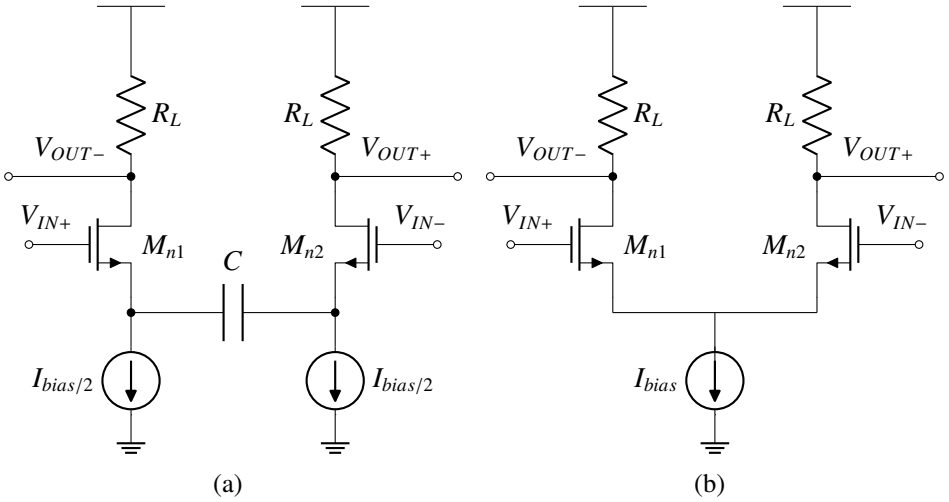


Figure 4.19: *(a) Split-source differential amplifier (b) Classical differential amplifier*

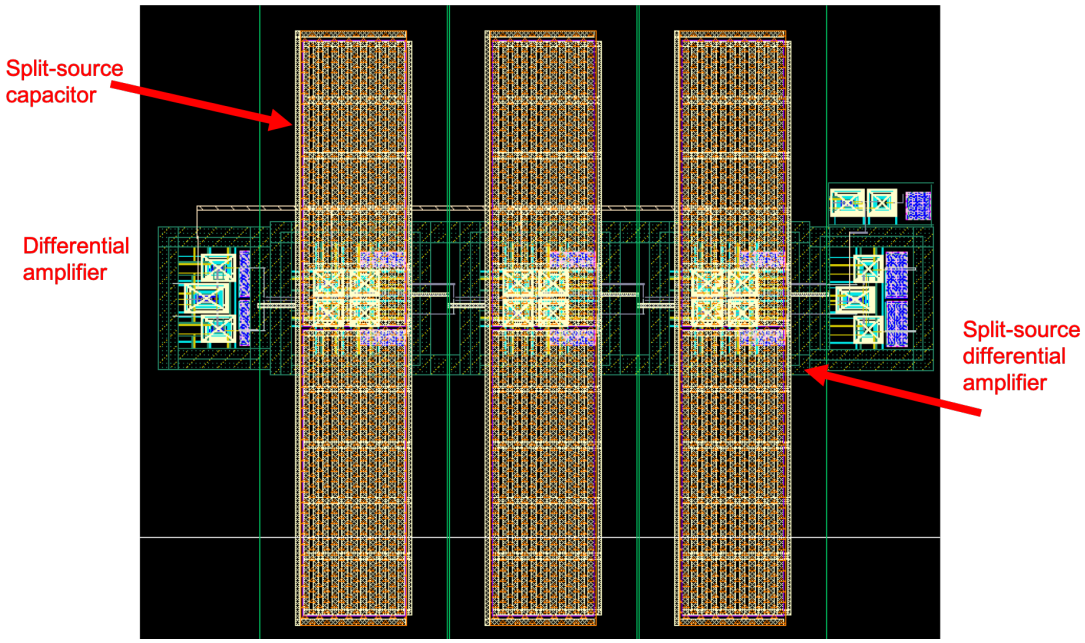


Figure 4.20: *Baseband amplifier layout*

4.4 Narrowband Correlator

The received information is encoded in PPM scheme, where the time-distance between two successive amplified envelope detected pulses represents logical zero or one. The NBC reduces the baseband bandwidth using multiple envelope detected pulses instead of one to implement the PPM scheme. It accumulates a train of successive envelope detected SAW correlator peaks, followed by a specific time-delay and then comes another train of successive pulses. The time-distance between the accumulated two pulse trains is used to encode the transmitted information as a PPM signal. Once the accumulated voltage of the NBC reaches a pre-defined level, a PPM digital signal is generated, which is used to reset all the parallel NBC units. Figure 4.23 demonstrates the NBC working principle,

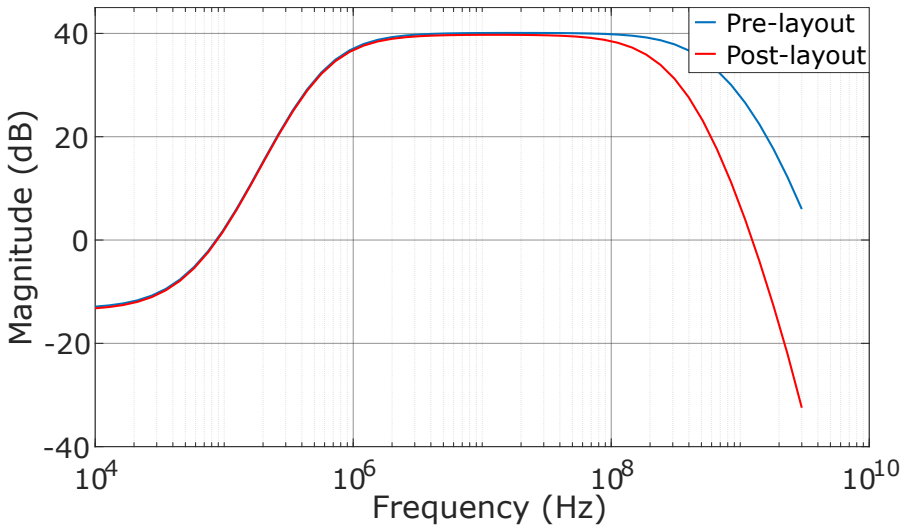


Figure 4.21: *Pre- and post-layout simulation of the baseband amplifier gain transfer function*

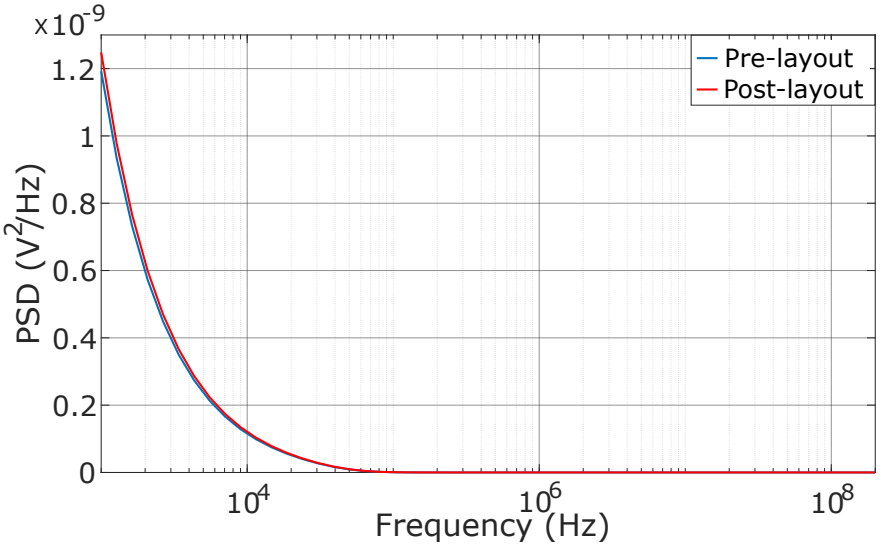


Figure 4.22: *Pre- and post-layout simulation of the baseband amplifier input-referred noise*

taking a train of 5 pulses as an example. Based on the time-domain output of the SAW correlator, the distance between each detected pulse is 238 ns, with 25 ns pulse width. In order to realize the concept of the NBC, parallel units of Operational Transconductance Amplifier (OTA) with Integrate-and-Hold Circuit (IHC) are used. The IHC is added to the OTA output to accumulate the voltage as a result of successive input pulses on the OTA. Since there is no synchronization between the transmitter and the WuRx, parallel units of the OTA with IHC are needed.

Figure 4.24 shows the NBC, which has 19 parallel units of OTA and IHC, with a driving clock duty-cycle of 25 ns. The output of each unit of the NBC enters a Schmidt trigger and then ORed in order to generate the PPM pulse that belongs to the highest accumulated NBC unit. The MPCG clocks are 50% interleaved in order to detect the input pulses

that come between two MPCG clocks, making the total amount of needed units 19. The number of parallel units is a result of dividing the waveform symbol length of 238 ns by 12.5 ns, which represents half of the duty-cycle of the generated MPCG clocks. To achieve this configuration, the period of the input clock of the MPCG equals to 476 ns. The input clock of the MPCG comes from a low-power PLL with external off-chip reference clock running at 32 kHz. The output frequency of the PLL is 2.097 MHz. The VCO is realized using current-starved inverter stages, which is a suitable oscillator design for low-power applications.

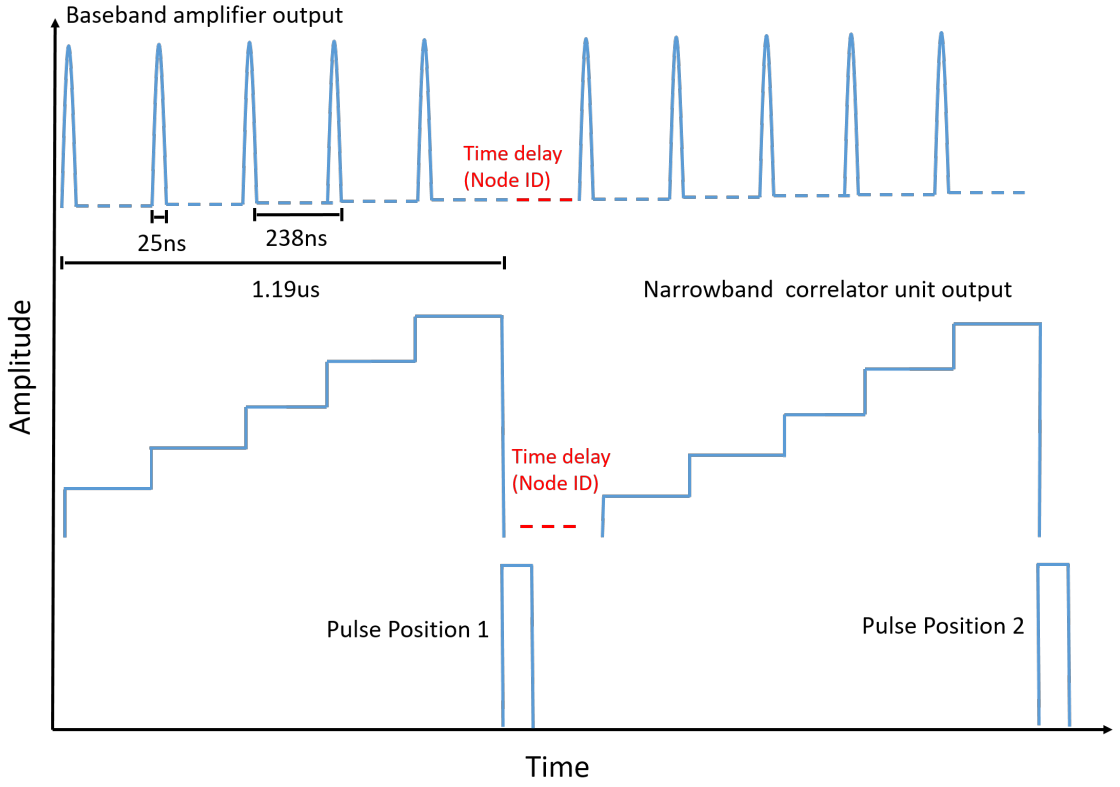


Figure 4.23: *NBC Working principle, implementing PPM demodulation scheme*

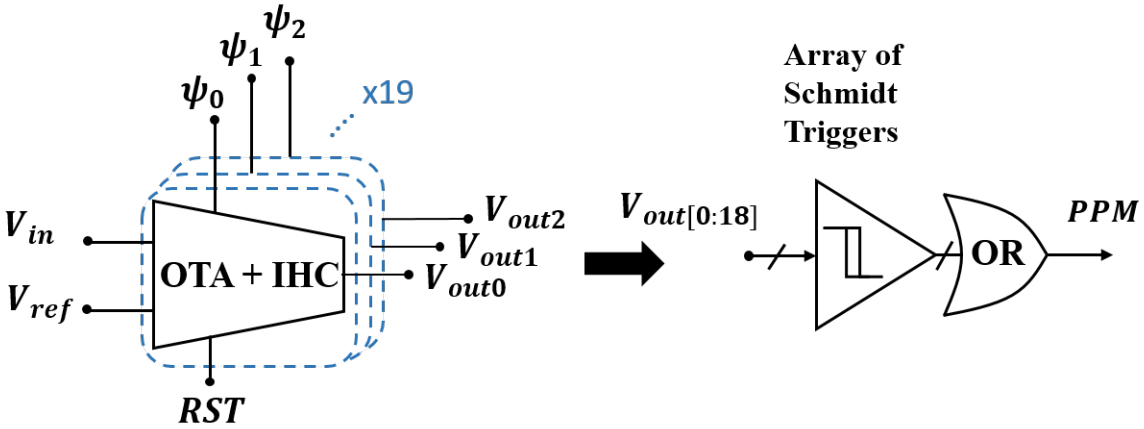


Figure 4.24: *NBC block diagram*

4.4.1 Operational Trans-conductance Amplifier (OTA) with IHC

Figure 4.25 shows the schematic of the used OTA with IHC. The amplified baseband signal enters one of the OTA inputs, while the other input is used as a DC reference to prevent noise floor accumulation. Figure 4.26 shows the layout of one unit of the OTA with IHC.

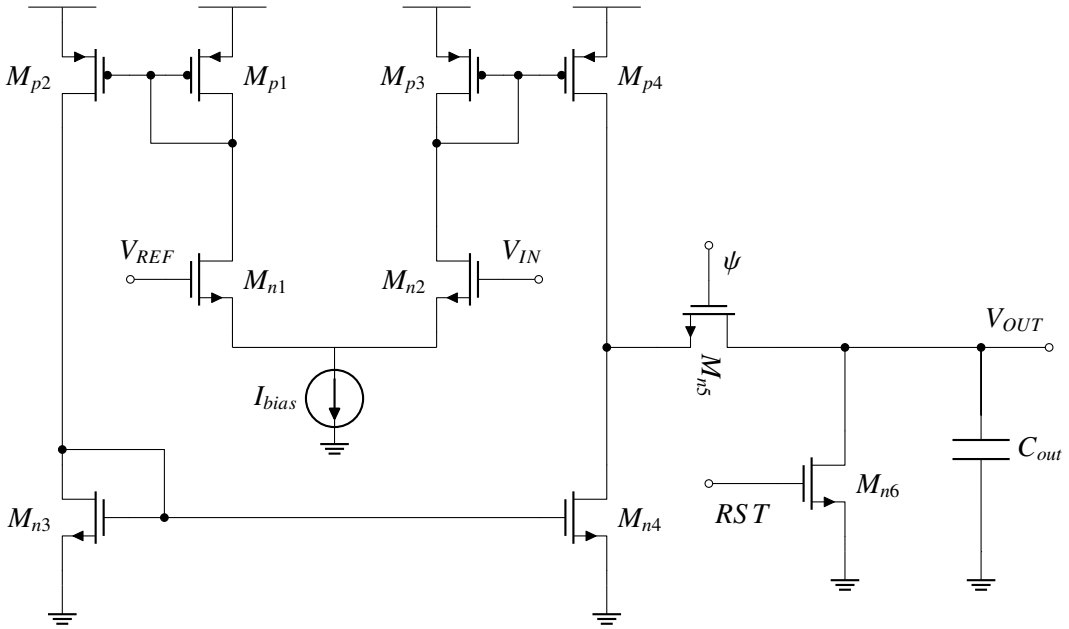


Figure 4.25: *Schematic of the OTA with IHC*

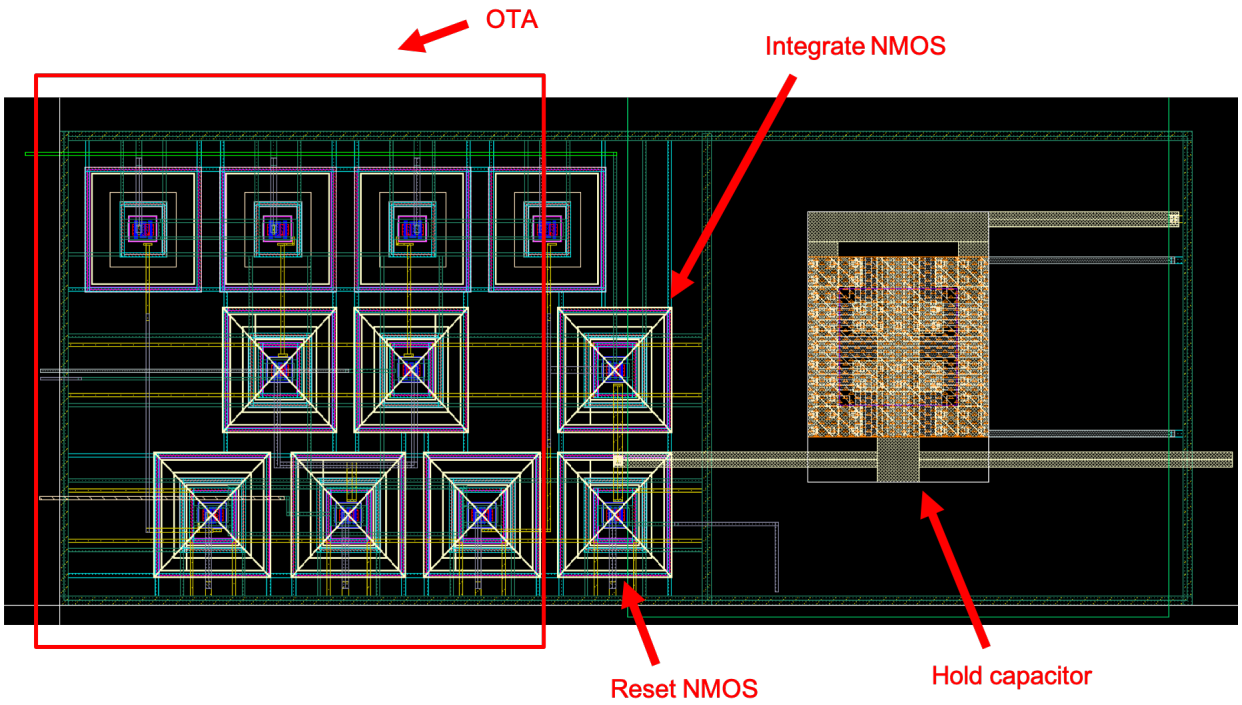


Figure 4.26: *layout of the OTA with IHC*

Figure 4.27 shows the pre- and post-layout simulated transfer function of the OTA, with a reduction of the amplification bandwidth in the post-layout due to the layout parasitics.

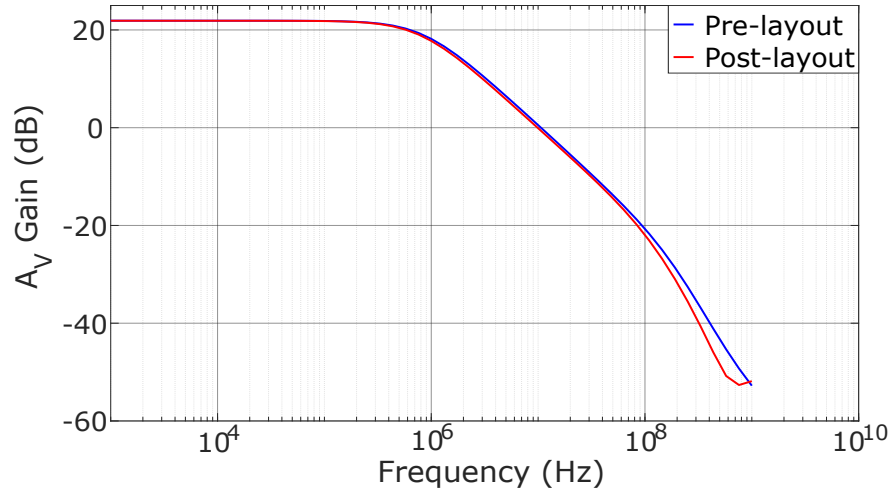


Figure 4.27: *Pre- and post-layout simulation for the OTA with IHC gain transfer function*

Figure 4.28 shows the pre- and post-layout simulation of one single unit of the NBC as a result of a 100 mV peak amplitude of the detected signal. The NBC unit accumulates four pulses before it reaches to a pre-defined voltage level, where the PPM pulse is generated. The accumulation time is 1 µs, which corresponds to a data-rate of 1 Mbps. While in Figure 4.29, the NBC unit needs to accumulate seven pulses in order to reach the same pre-defined PPM generation level, making the data-rate 600 kbps with an increase in the receiver sensitivity versus data-rate reduction. In the two figures, the step wave time equals to the SAW detected pulse wave time, which is 238 ns.

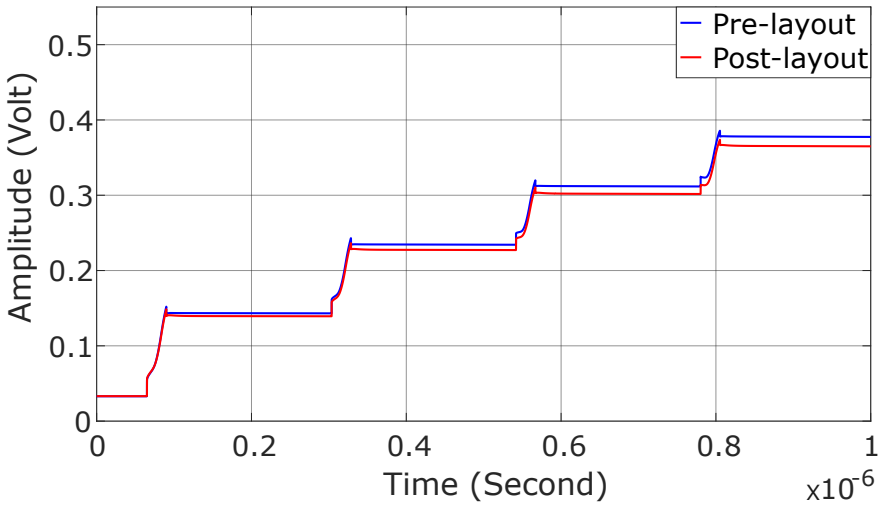


Figure 4.28: *Pre- and post-layout simulation of the NBC unit output as a result of 100 mV baseband signal*

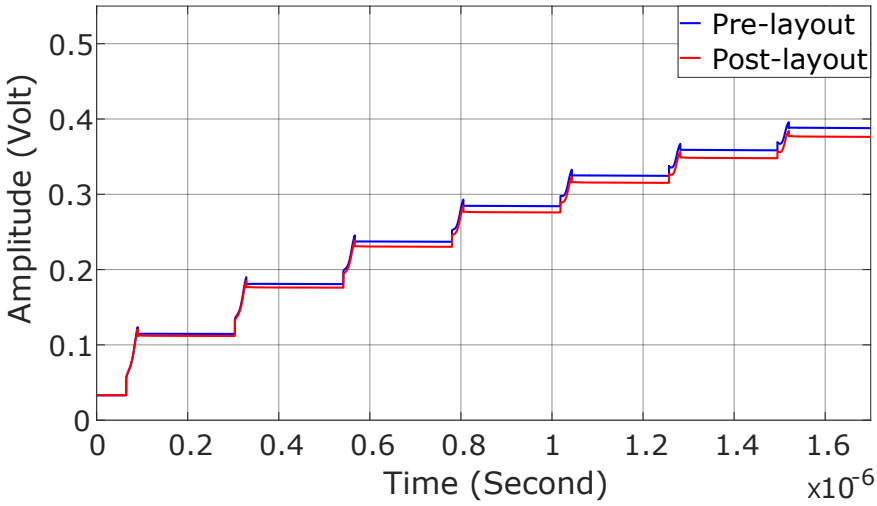


Figure 4.29: *Pre- and post-layout simulation of the NBC unit output as a result of 50 mV baseband signal*

4.5 Multi-Phased Clock Generator

Figure 4.30 shows the block diagram of the MPCG. The MPCG is driven by the PLL output and it consists of 19 delay units. The output of the delay units are XORed in order to generate the phase difference between the delay cells. As an example, in order to generate inter-leaved phased clocks, the delay $cell_1$ output is XORed with $cell_3$.

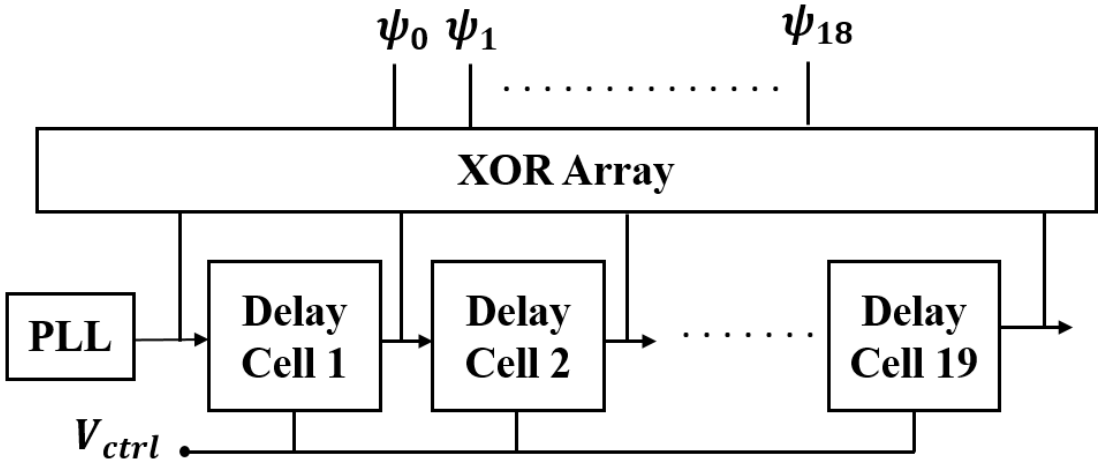


Figure 4.30: *MPCG block diagram*

The schematic of the single delay cell is shown in Figure 4.31. The unit is based on current-starved delay line that allows for low-power design. Figure 4.32 shows the pre- and post-layout simulation of the MPCG cell delay with respect to the input control voltage. The target delay for each cell is 25 ns, which corresponds to a control voltage of 800 mV.

Figures 4.33 and 4.34 shows the pre- and post-layout simulation of the first and the last phase generated by the MPCG. The last phase of the MPCG exhibits a duty-cycle error,

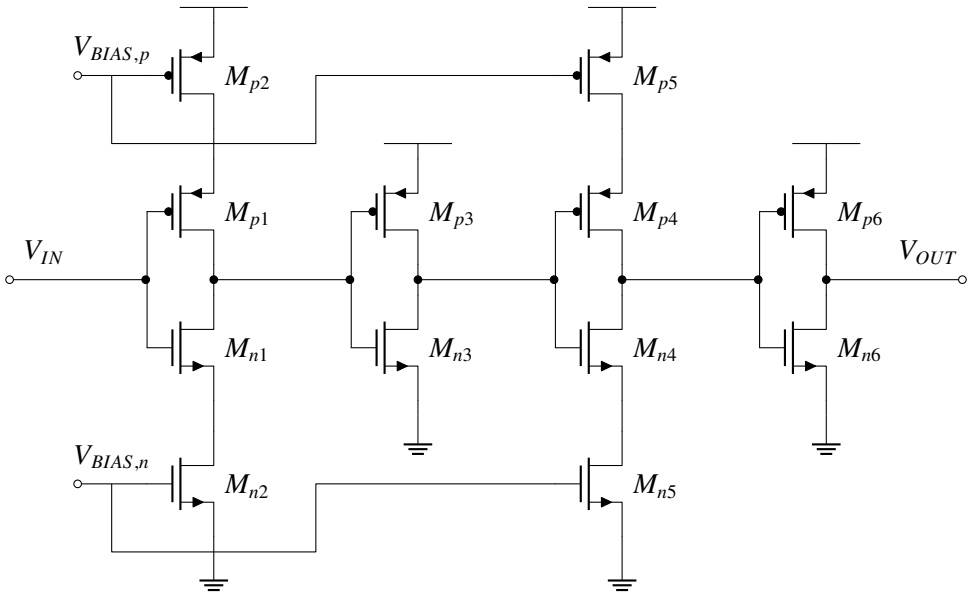


Figure 4.31: *Schematic of the voltage-controlled delay cell*

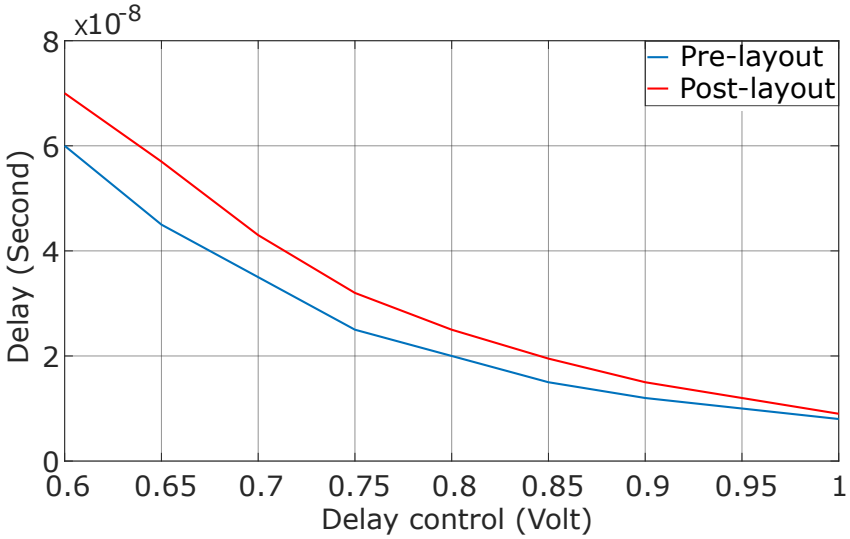


Figure 4.32: *Pre- and post-layout simulation of single MPCG delay cell vs. input control voltage*

which can be corrected by means of duty-cycle correction circuits, however, this leads to a significant increase in the amount of power dissipation.

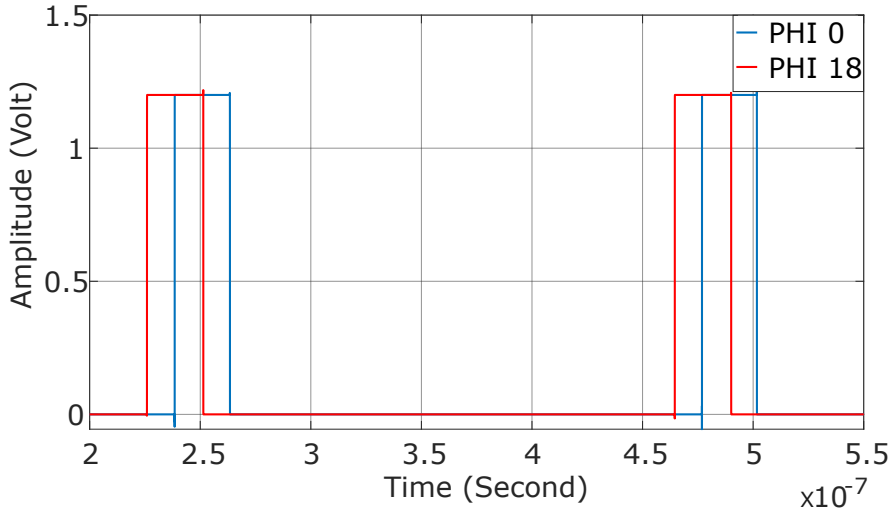


Figure 4.33: *Pre-layout simulation for phase 0 and 18*

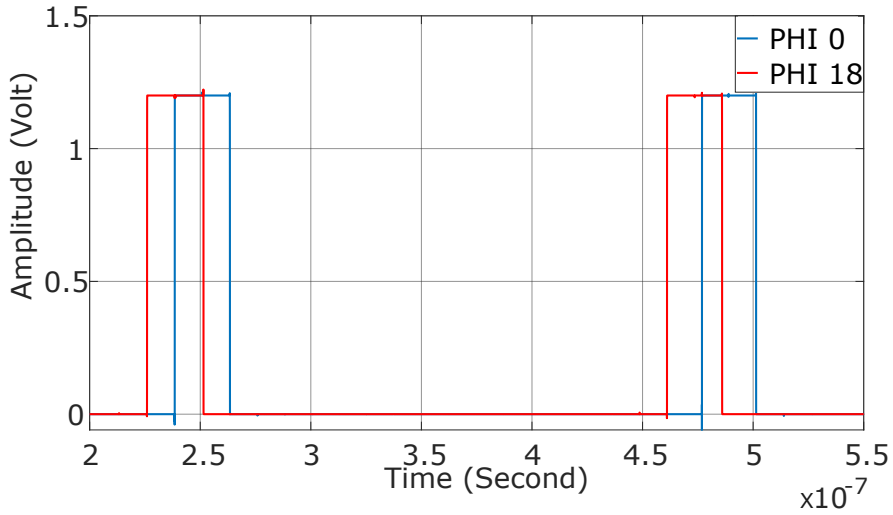


Figure 4.34: *Post-layout simulation for phase 0 and 18*

4.6 Phase Lock Loop

Figure 4.35 shows the PLL block diagram. The PLL reference clock is 32 kHz, and a loop divider of 64, which makes the output frequency equals to 2.097 MHz. The PLL is based on three-state Phase Frequency Detector (PFD). The output of the PFD triggers the Charge Pump (CP), where the difference in phase and frequency is converted to voltage in the loop filter. The Voltage Controlled Oscillator (VCO) is based on current-starved inverter stages to allow for low-power dissipation design as shown in Figure 4.36. The VCO consists of

11 stages. The number of stages, current and gate-oxide thickness determines the output frequency.

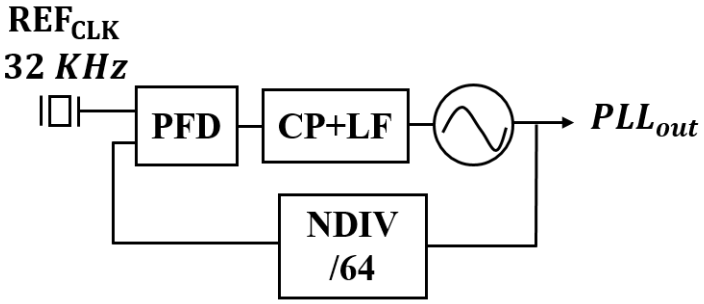


Figure 4.35: *PLL block diagram*

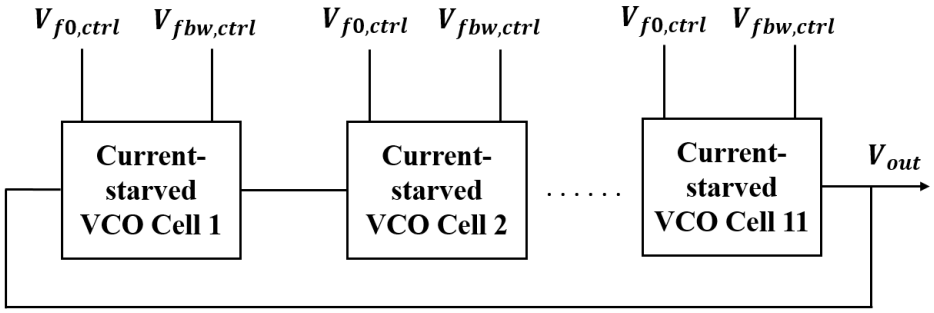


Figure 4.36: *Current-starved VCO block diagram*

The VCO inverter stage schematic is shown in Figure 4.37. The VCO has two control signals, one comes from the PLL LF and the other is an external manual input to control the VCO center frequency.

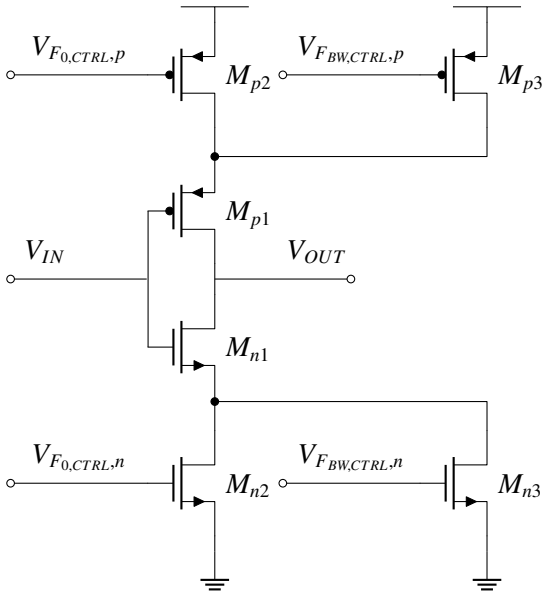


Figure 4.37: *Schematic of current-starved VCO stage*

Figure 4.38 shows the VCO pre- and post layout simulation for the frequency change with respect to the input control voltage, where the VCO frequency changes between 0.4-0.9 volts.

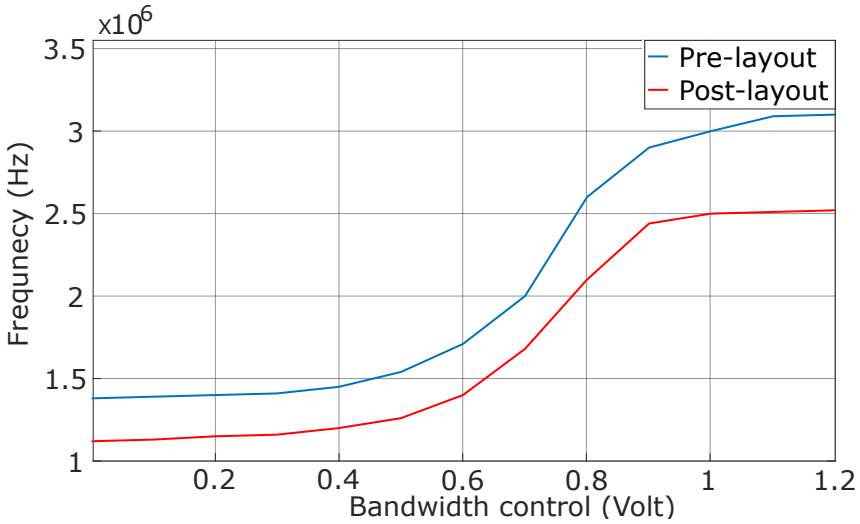


Figure 4.38: *VCO output frequency vs. control voltage*

4.7 WuRx Chip Layout

Figure 4.39 shows the complete WuRx IC layout, where the IC major sub-components are labeled. The dimensions of the chip with the pads are 1117 µm x 920 µm.

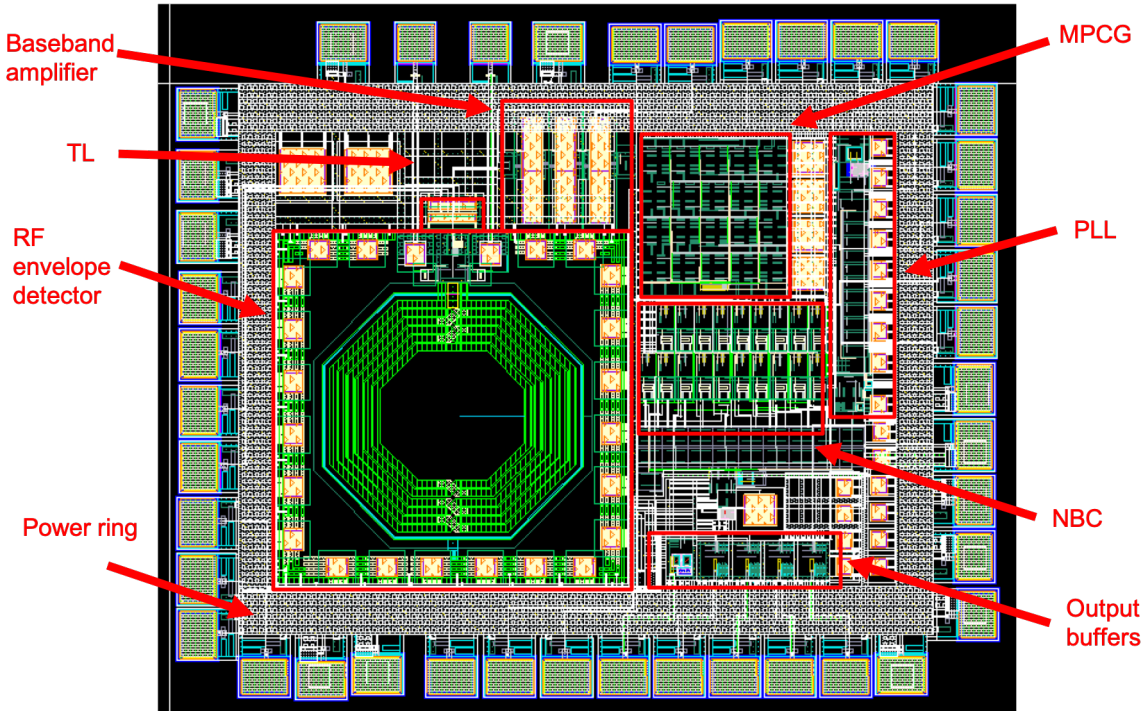


Figure 4.39: *WuRx IC layout*

4.8 Summary

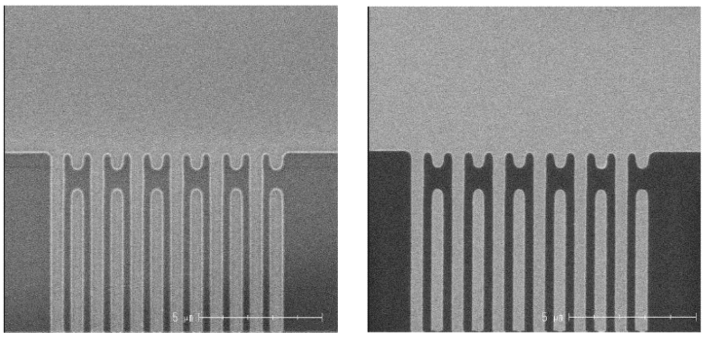
This chapter presents the design, implementation and simulation of the major sub-components of the WuRx IC, with a focus on the SAW correlator and the RF detector. The chapter also explains from the system perspectives the baseband signal processing, where the baseband bandwidth is reduced by means of a NBC and a PPM demodulation scheme. In the next chapter, the measurements of the designed IC are reported.

5 Results and Measurements

This chapter reports the WuRx measurements. The chapter starts with a brief summary of the SAW correlator fabrication process. Subsequently, the device characterization in both time and frequency domain are reported. To validate the concept of the co-channel interference robustness technique provided by the SAW correlator, a direct-detection receiver with discrete devices is designed, fabricated and measured. Following the SAW correlator measurements, the WuRx IC measurements are presented. The section reports the measurements of each subsystem of the WuRx, starting with the RF envelope detector and baseband amplifier, then the NBC, PLL and MPCG measurements. The chapter ends with the simulation of a proposed digital processing block based on measured data obtained from the NBC. The digital processing unit demonstrates the transmitted node ID demodulation, and the wake-up signal assertion.

5.1 SAW Correlator

The device operates at 2.44 GHz centered ISM band, with 50 Ω input and output ports impedance. Figure 5.1 demonstrates the IDT finger pairs fabrication for a set of 6 IDT pairs.



(a) (b)

Figure 5.1: *(a) Photo-resist in-situ mask, dark zones correspond to the resist pattern [8], [A1] (b) Metal deposited on the substrate after lift-off, dark zones correspond to the substrate surface [8], [A1]*

The wavelength is considered 1.6 µm for Lithium Niobate $LiNbO_3$ substrate with 50% metalization ratio, and electrode width of 400 nm. 2% Cu doped Aluminum metal patterned fabricated using lift-off technique. The patterned photo-resist layer is placed on $LiNbO_3$ substrate using a Nikon i-line Body-9 stepper. The pattern is transferred from a 5-scale reticle using photo-reduction. The photo-resist mask is covered with metal using a calibrated evaporation process to allow for better layer thickness than ±2% as shown in Figure 5.1(a). Following the IDT pairs lift-off, the contact pads are reloaded to ease the wire bonding process as shown in Figure 5.1(b). The device is then diced and placed in Surface Mounting Packages (SMP), so it is easier to mount on PCB. Figure 5.2 shows

a bare sample of the fabricated SAW correlator with a total area of 3 mm^2, achieving a small device size that fits properly in the SMP [8], [A1].

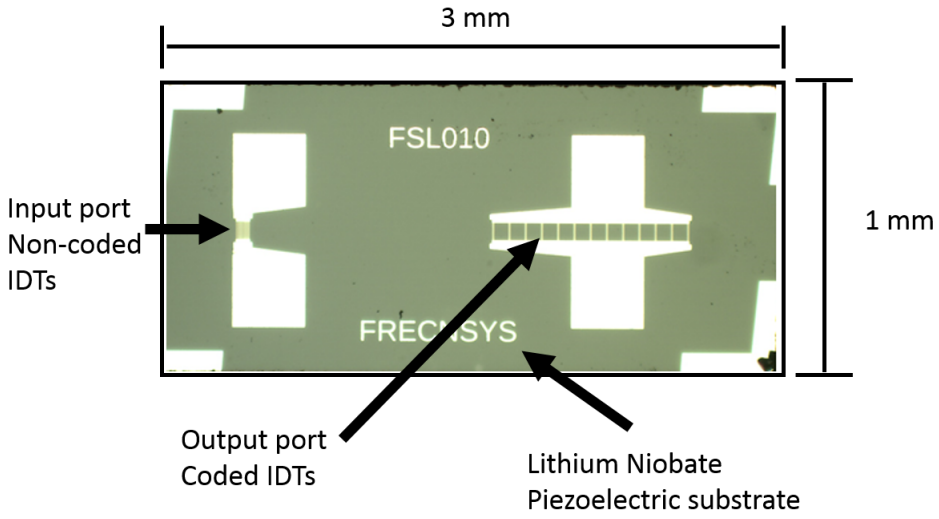


Figure 5.2: *Bare sample of the fabricated 13-bits 2.44 GHz BPSK Barker-coded SAW correlator [8], [A1]*

5.1.1 Time and Frequency Domain Measurements

Figure 5.3 shows the block diagram of the time-domain measurements setup for the SAW correlator as the Device Under Test (DUT). The input excitation signal scheme is programmed in GNUradio, which is an open-source programming environment for Software Defined Radios (SDR). The input signal consists of 13-bits BPSK Barker-coded signal at 2.42 GHz, according to the signal synthesis described in Chapter 4.

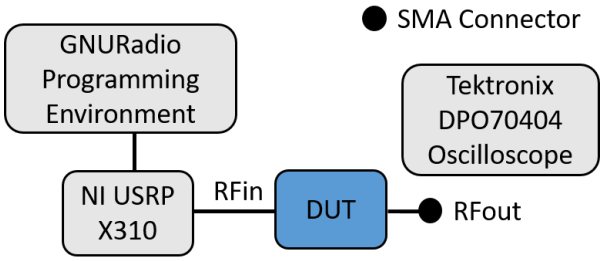


Figure 5.3: *Block diagram of the SAW correlator time-domain measurements setup*

The programmed signal is then generated using the National Instruments Universal Software Radio Peripheral (NI USRP) X310. The device operates from DC up to 6 GHz, with a bandwidth of 120 MHz. The output signal is probed on Tektronix DPO70404 oscilloscope, which has a 4 GHz sampling bandwidth. From the SAW correlator measurements in frequency-domain, the device exhibits a frequency shift of 20 MHz and operates optimally at 2.42 GHz instead of 2.44 GHz. Figure 5.4 shows the single input/output SAW correlator placed inside a high frequency SMP and mounted on a PCB with external series inductor for output port impedance matching.

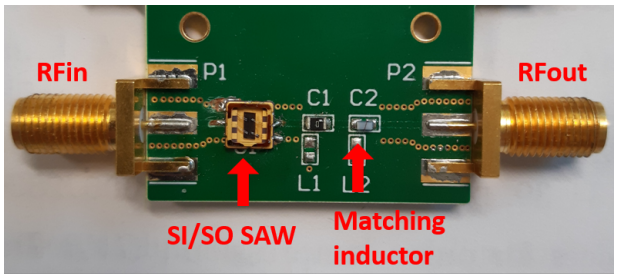


Figure 5.4: *DUT- SI/SO SAW correlator placed in SMP and mounted on an RF PCB*

Figure 5.5 shows the measured input and output reflection parameters S_{11} and S_{22} for the DUT in Figure 5.4. Both ports are matched to 50 Ω at 2.42 GHz, with the use of serial inductor at the output port.

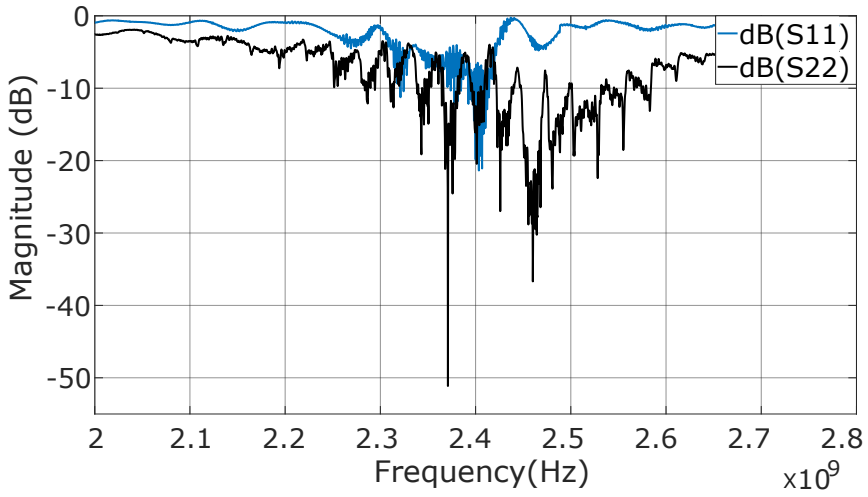


Figure 5.5: *Measured SAW correlator input/output reflection coefficients*

The SAW correlator measured transfer function S_{21} is shown in Figure 5.6. The device exhibits a power loss of 12 dB at 2.42 GHz, which matches the device simulation. The SMP introduces a pole at 2.45 GHz, which reduces the bandwidth of the device. Figure 5.7 shows the measured time-domain output of the SAW correlator, as a result of 13-bits 2.42 GHz BPSK Barker-coded input signal. The device has a clear RF pulse, with total amplitude compression gain of $A_v = 0.42$ (after device IL), which is is equivalent to 5 −6 dB of amplitude compression gain. The time distance between each two successive RF pulses is 238 ns, with each pulse width equals to 25 ns.

5.1.2 Co-channel Interference Robustness

A PCB based RF direct-detection receiver is designed to validate the concept of co-channel interference robustness provided by the SAW correlator. Figure 5.8 shows the block diagram of the measurement setup used for validating the co-channel interference robustness. The receiver PCB is composed of an SAW correlator package, an RF enve-

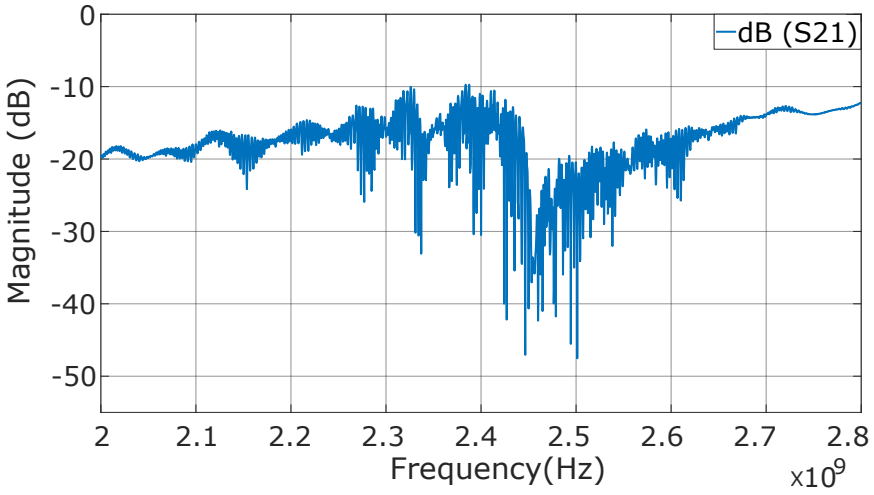


Figure 5.6: *Measured SAW correlator transfer function* S_{21}

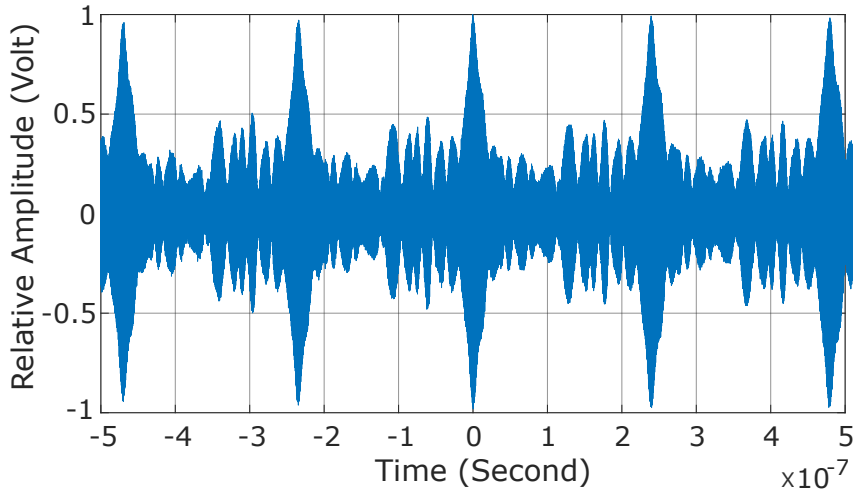


Figure 5.7: *Measured SAW correlator relative time-domain output*

lope detector realized using Schottky diode, and a 100 MHz wideband baseband amplifier as shown in Figure 5.9.

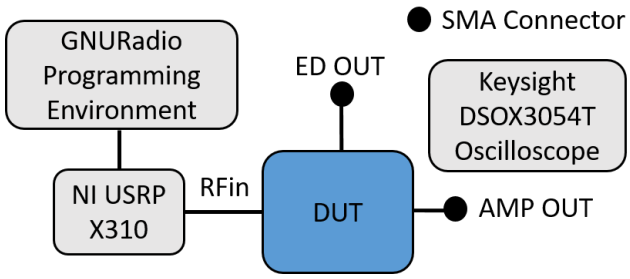


Figure 5.8: *Block diagram of the co-channel interference robustness measurements setup*

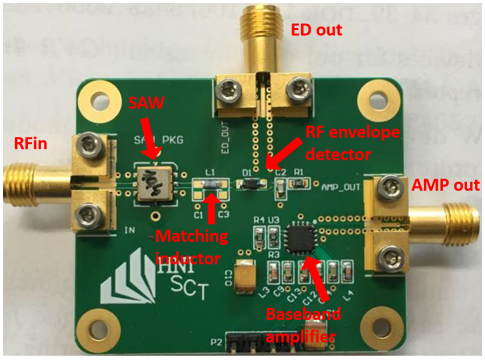


Figure 5.9: *DUT- PCB of direct-detection receiver made from discrete devices*

Figure 5.10 shows that the detected and amplified output signal as a result of 13-bits 2.42 GHz BPSK Barker code excitation signal is almost 5 −6 dB larger, compared with the detected and amplified WiFi output or sine wave signal at 2.42 GHz.

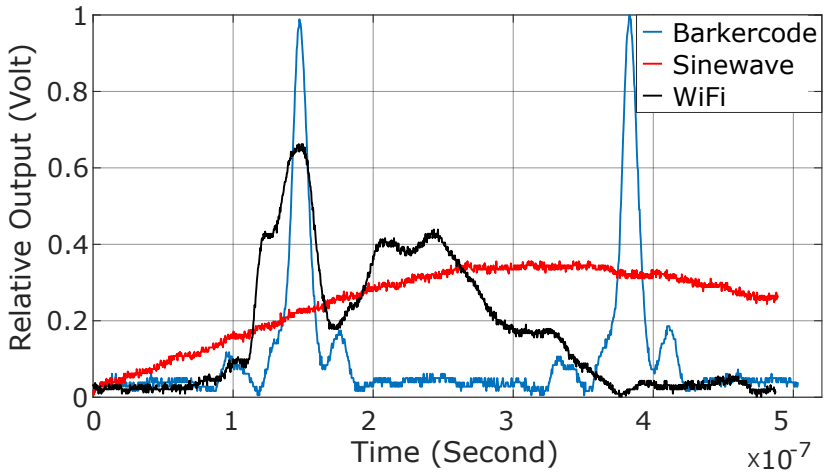


Figure 5.10: *Measured discrete elements PCB output as a result of 13-bits BPSK Barker code, WiFi and sine wave input signals at 2.42 GHz*

5.2 WuRx Integrated Circuit

This section reports the WuRx IC measurements. The section starts with the RF front-end and baseband amplification measurements, and then reports the measurements of the NBC, PLL and MPCG.

5.2.1 Front-end and Baseband Amplification

Since the used RF envelope detector designed in Chapter 4 has differential-inputs, the SAW correlator output is converted from single-end to differential using an RF balun as shown in Figure 5.11. The RF balun input and output ports are matched to 50 Ω and operates from 2.3 GHz to 2.6 GHz, with an IL less than 1 dB.

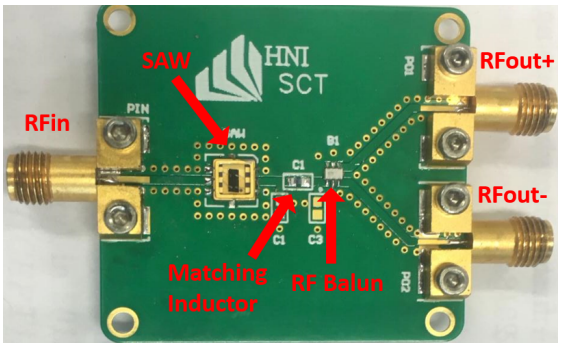


Figure 5.11: *Single-input/differential-output SAW correlator RF PCB*

The block diagram of the front-end measurements setup is shown in Figure 5.12. The SAW correlator PCB is connected to the differential-inputs of the front-end PCB using RF coaxial cables.

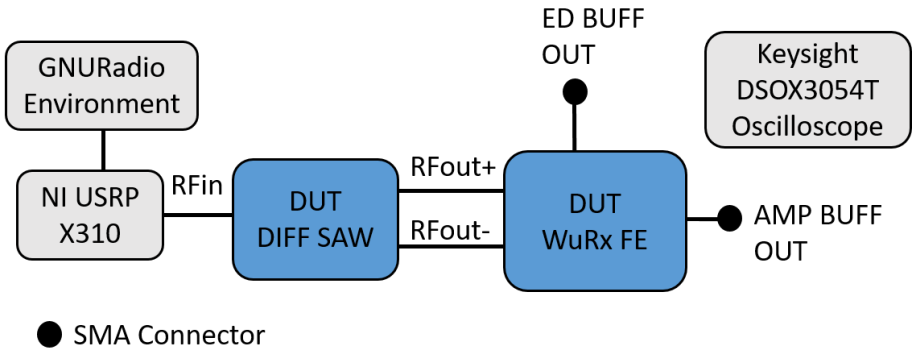


Figure 5.12: *Block diagram of the WuRx front-end measurements setup*

Figure 5.13 shows the front-end PCB with the WuRx chip mounted and bonded on it. The DUT also consists of the input impedance matching network for the RF envelope detector, in addition to the dip-switches that configure the RF envelope detector biasing current, and are used to enable/disable the output 50 Ω buffers for the RF envelope detector and the baseband amplifier. The PCB is connected to the power management board to provide

the supply voltage and the DC biasing points. The power management board details are explained later in this chapter. Figure 5.14 shows the measured S_{11} at 2.42 GHz, using an external matching network.

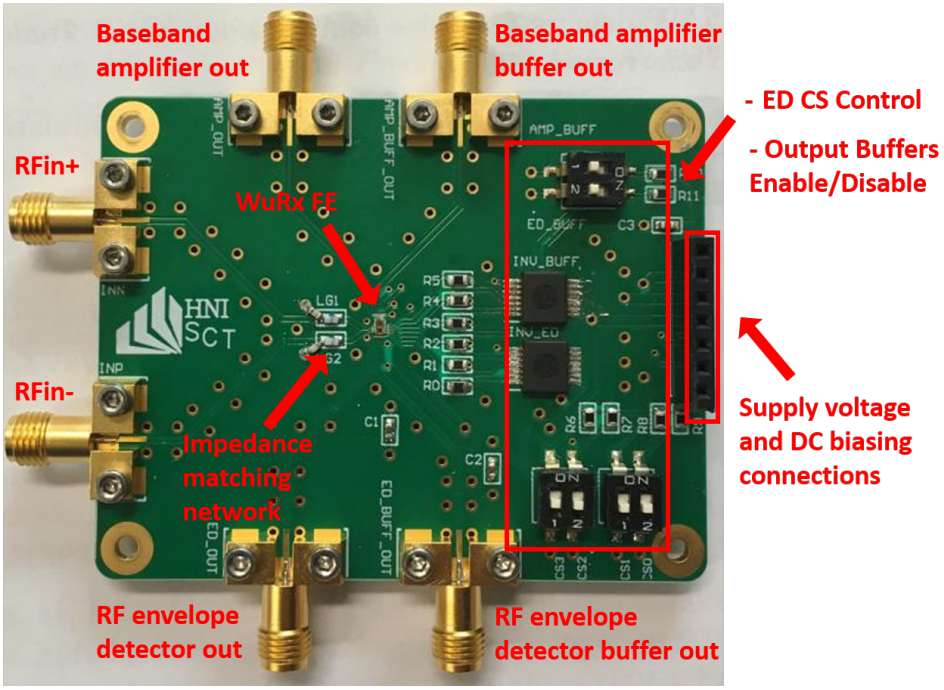


Figure 5.13: *DUT- WuRx front-end RF PCB*

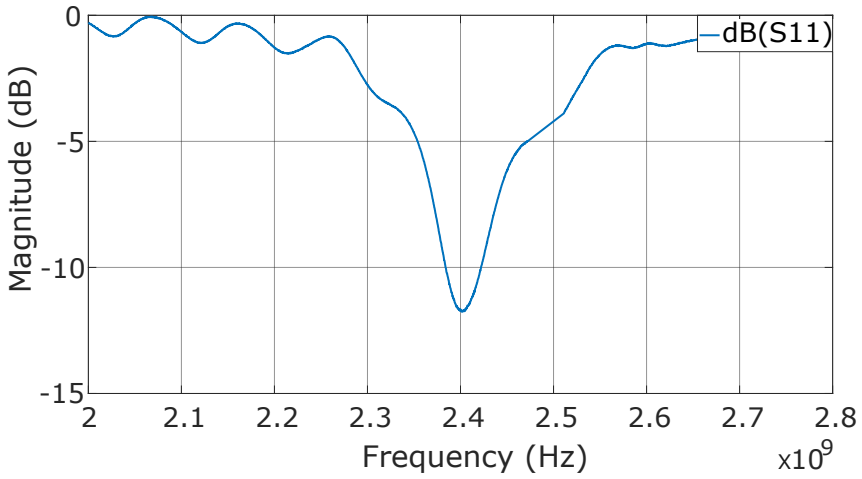


Figure 5.14: *Measured RF envelope detector input reflection coefficient*

The measured time-domain output of the RF envelope detector is shown in Figure 5.15, where an enveloped version of the output RF pulses of the SAW correlator is produced, with a 180° signal phase shift between the input and the output. The RF envelope detector dissipates 12 µA from 1.2 V supply voltage. The measured time-domain envelope detection shows a reduction in the detected pulse width, which comes from the reduction in the bandwidth of the RF envelope detector low-pass filter. However, the time-distance

between the peaks of the detected pulses is constant and equal to 238 ns. The RF envelope detector conversion gain versus the input amplitude is shown in Figure 5.16. The plot shows that the conversion becomes almost linear after 4 mV differential-input amplitude, where the RF envelope detector input transistor starts to operate in the saturation region.

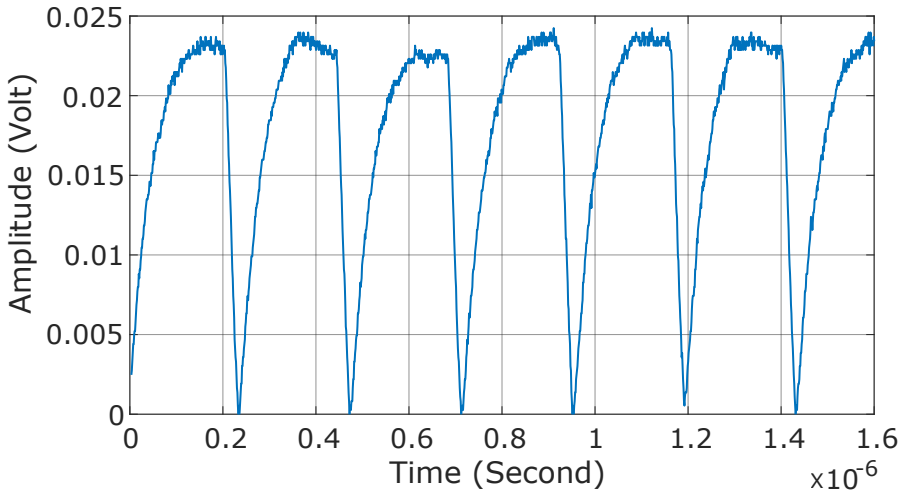


Figure 5.15: *Measured RF envelope detector time-domain output at −24 dBm SAW input power*

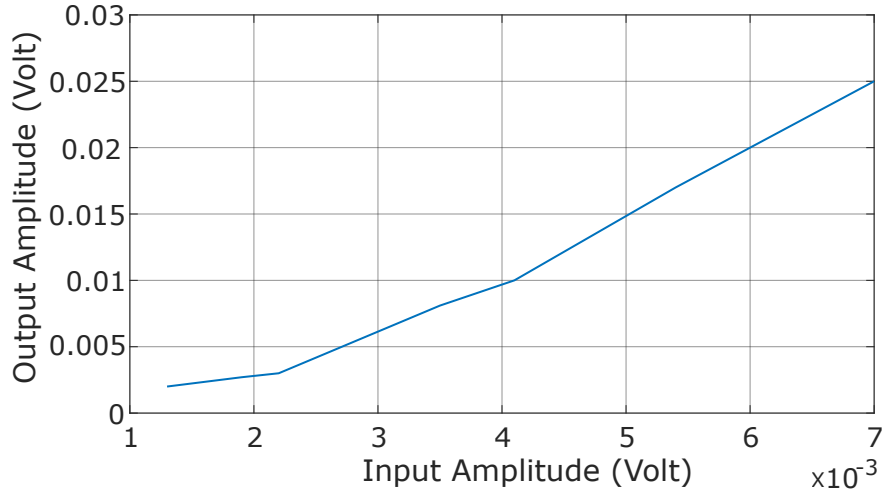


Figure 5.16: *Measured RF envelope detector conversion gain vs. input amplitude*

Figure 5.17 shows the measured time-domain output of the baseband amplifier for a 4 mV input peak signal. The measured baseband amplifier achieves a gain of 35 dB. The pulse width is further increased due to the reduction in the measured baseband amplifier bandwidth. However, the output shows a clear pulse, with pulse distance equals to 238 ns. The baseband amplifier dissipates 65 µA from 1.2 V supply voltage.

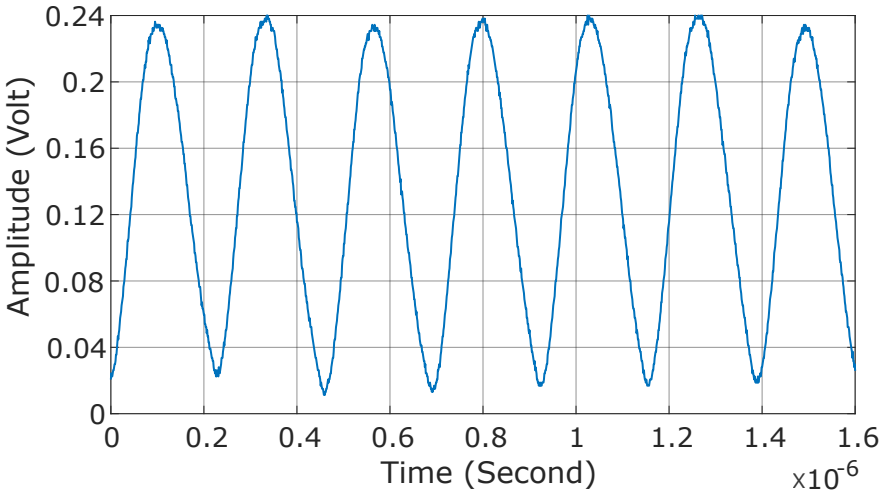


Figure 5.17: *Measured baseband time-domain output for 4 mV input signal*

5.2.2 Narrowband Correlator

Figure 5.18 shows the block diagram of the measurements setup for the WuRx baseband processing, with the NBC, PLL and MPCG 50 Ω buffers. The SAW correlator PCB is connected with RF coaxial cables to the differential-inputs of the RF envelope detector.

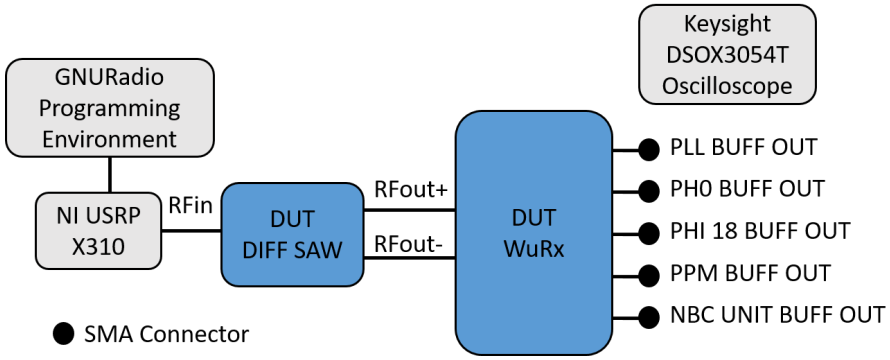


Figure 5.18: *Block diagram of the WuRx chip measurements setup*

The DUT is shown in Figure 5.19, where the PCB subsystems are marked. The DUT has 32 kHz quartz oscillator as a reference clock for the PLL, where the PLL second order loop filter is realized externally. The RF envelope detector is biased in different regions using the configuration dip-switches as explained in Chapter 4. Additionally, the chip output buffers are externally enabled/disabled. Similar to the WuRx front-end DUT, the PCB is connected with a power management board to provide the supply voltage and the DC biasing points.

Figure 5.20 shows the output of one of the NBC units, where it accumulates two successive detected and amplified SAW correlator output, providing a total receiver sensitivity of −44 dBm at a data-rate of 2 Mbps, with a sensitivity enhancement of 7 dB compared to the front-end sensitivity of −37 dBm. The NBC units are reset using the digital PPM signal when the accumulated voltage reaches a pre-defined level. The receiver sensitivity is further improved when further reducing the baseband bandwidth, and hence lower

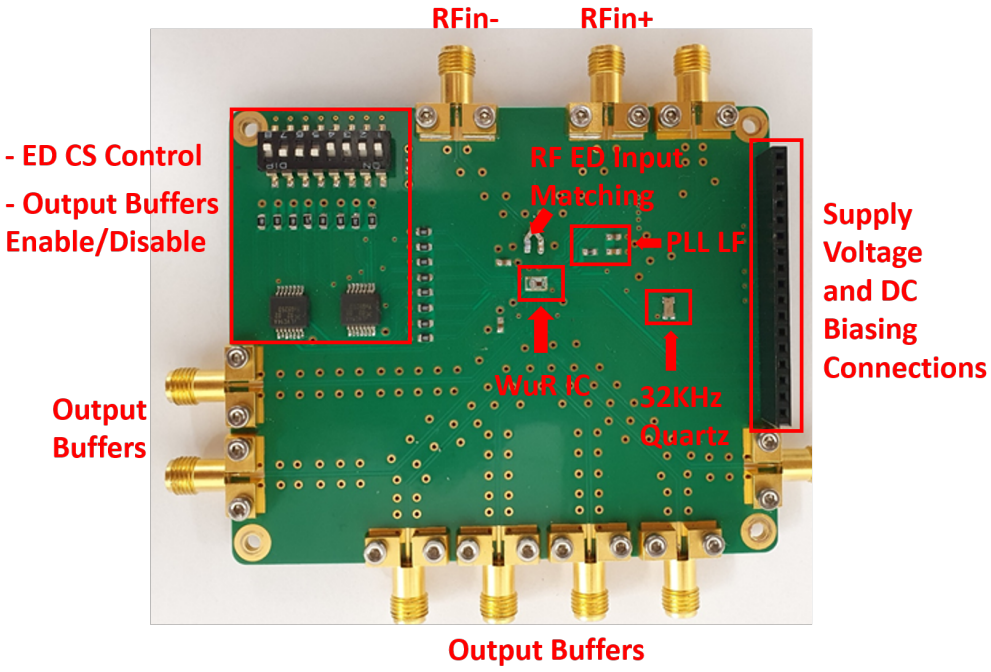


Figure 5.19: *DUT- Complete WuRx RF PCB*

communication data-rate is achieved. Figures 5.21, 5.22 and 5.23 show different outputs of the same NBC unit, with reduced data-rate and improved sensitivity. Figure 5.23 accumulates seven successive detected and amplified SAW correlator output, providing a total receiver sensitivity of −50 dBm at a data-rate of 600 kbps, with 13 dB sensitivity enhancement. The −50 dBm is the maximum sensitivity achieved in this measurement due to the baseband amplification limit.

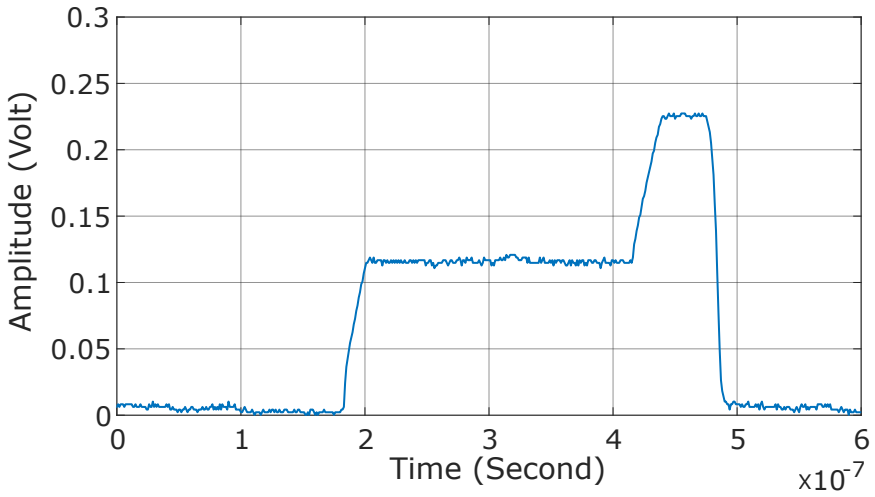


Figure 5.20: *Measured NBC unit time-domain output at −44 dBm SAW average input power and a data-rate of 2 Mbps*

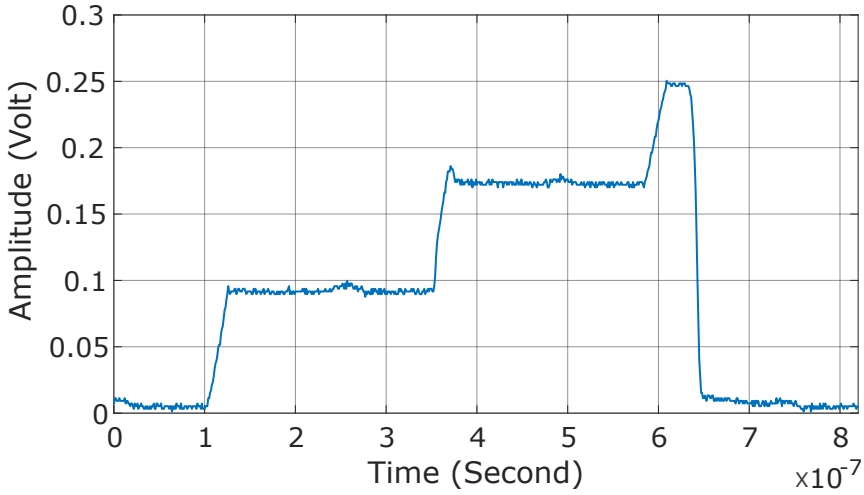


Figure 5.21: *Measured NBC unit time-domain output at −46 dBm SAW average input power and a data-rate of 1.5 Mbps*

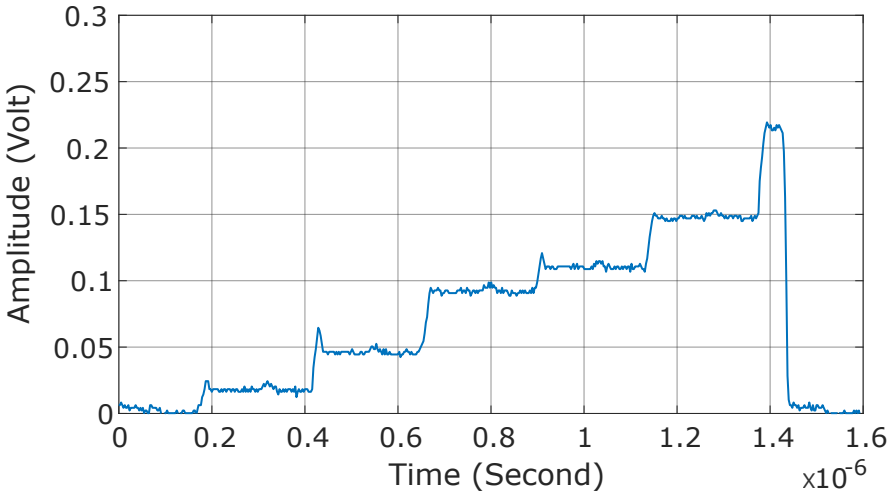


Figure 5.22: *Measured NBC unit time-domain output at −48 dBm SAW average input power and a data-rate of 670 kbps*

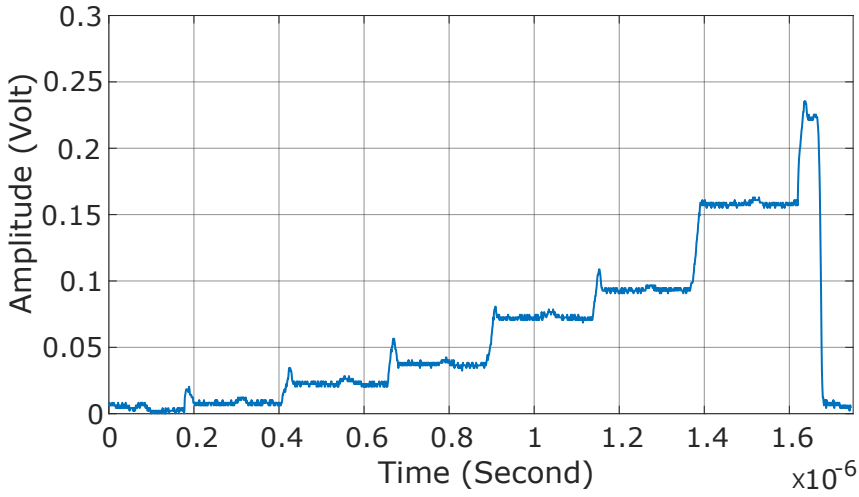


Figure 5.23: *Measured NBC unit time-domain output at −50 dBm SAW average input power and a data-rate of 600 kbps*

5.2.3 PLL and MPCG

The NBC needs to be driven by an MPCG, where it is also driven by a 2.097 MHz PLL. Figure 5.24 shows the measured PLL time-domain output with 50% duty-cycle. Figure 5.25 shows the measured frequency-domain output of the PLL, where it is locked at 2.097 MHz.

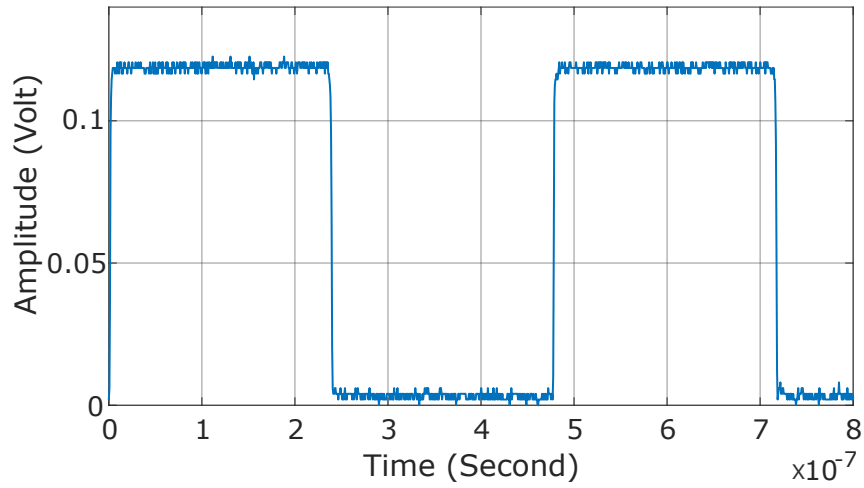


Figure 5.24: *Measured PLL time domain output*

The designed MPCG has 19 phased-clocks, where only two are probed for measurements. Figure 5.26 shows the first and the last phased-clocks, with 50% overlapping. The measurements show a duty-cycle error in the last phased-clock, which can be corrected using duty-cycling correction circuits, however this adds additional power and is not considered in this design.

The full WuRx dissipates 142 µW. The distribution of the measured power dissipation of

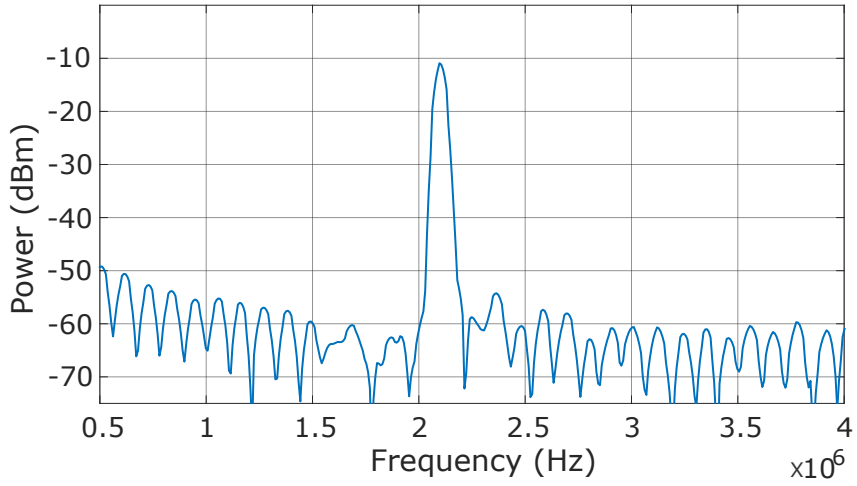


Figure 5.25: *Measured PLL output spectrum*

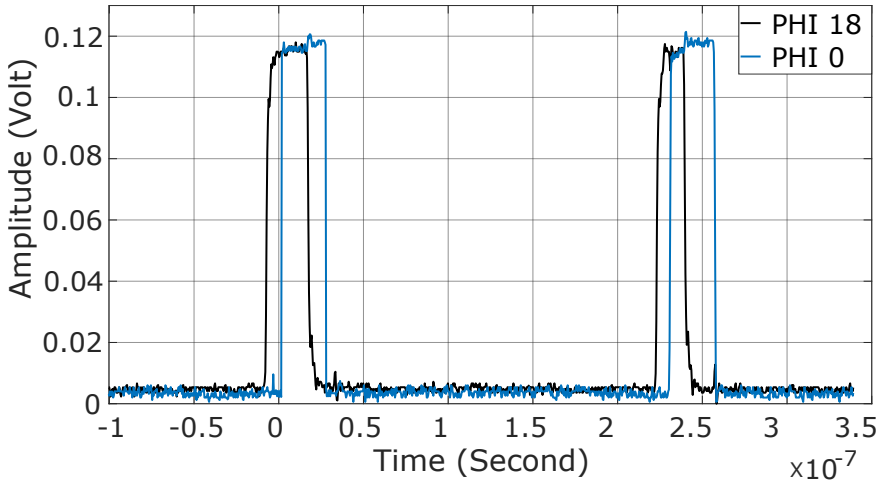


Figure 5.26: *Measured MPCG time domain output phase 0 and 18*

the chip is shown in Figure 5.27, where the baseband amplifier dissipates almost half of the power budget, due to it's high gain and wide bandwidth.

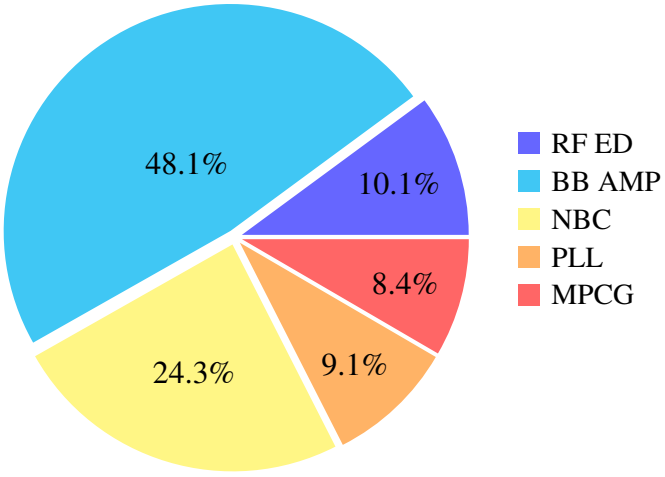


Figure 5.27: *Measured power dissipation distribution*

Figure 5.28 shows the WuRx chip micro-photograph with marked IC subsystems. The chip area with pads and output buffers is 1.02 mm^2, which complies with the design target.

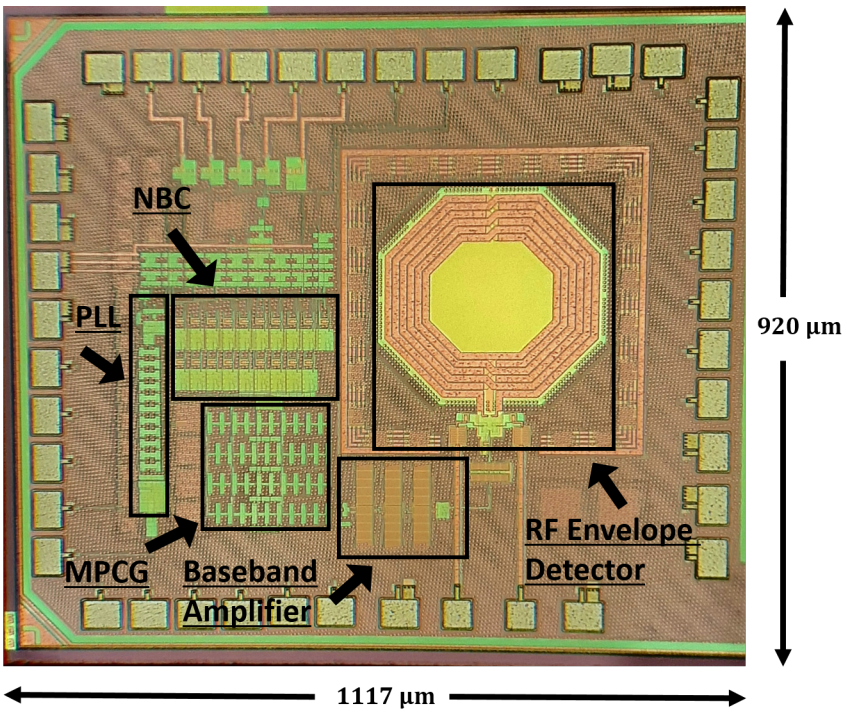


Figure 5.28: *Full WuRx IC Micro-photograph*

5.3 Power Management Board

Figure 5.29 shows the power management broad. The board provides the supply voltage to the chip core and the buffers with separate supply voltage. In addition, the board provides the needed DC biasing points such as the baseband amplifier and the NBC input reference voltages. The board is connected using bridge of connectors to the DUT. Each DC point is composed of Low-dropout Regulator (LDO), with a potentiometer to provide manual adjustments for the output voltage.

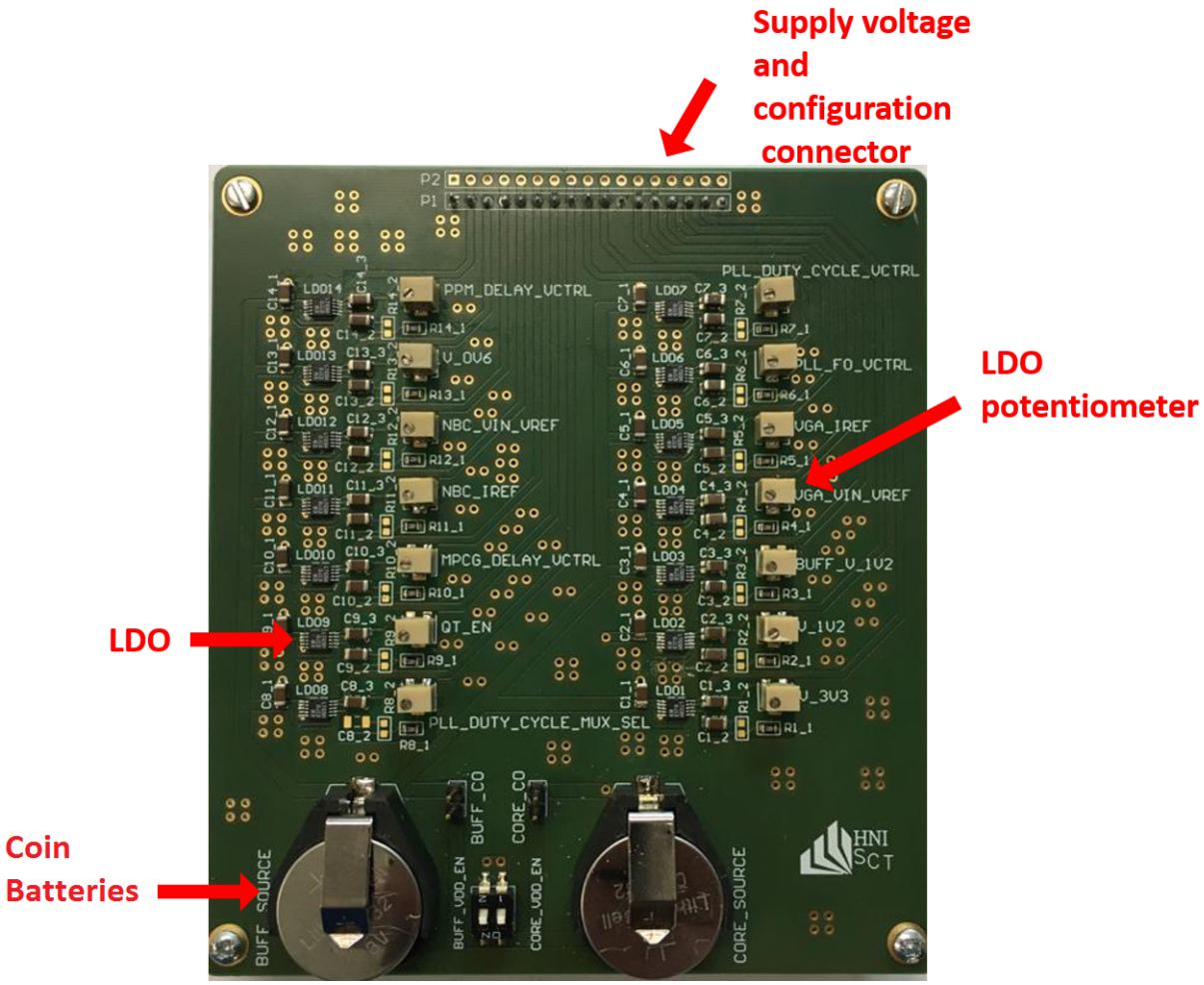


Figure 5.29: *Power management PCB*

5.4 Digital Processing

The proposed digital processing unit is shown in Figure 5.30. The digital processing unit is not fabricated in this thesis, however, its simulation is based on measured inputs from the NBC, where the transmitted node ID is encoded as a PPM scheme. The proposed design is composed of array of 19 Schmidt trigger circuits, which are ORed to generate the digital node ID as a PPM scheme. The generated digital PPM signal is fed to a C-element circuit to synchronize with the clock that drives the counter block. The PPM node

ID is decoded using a counter, where every PPM digital signal resets it. Depending on the counted value of the counter, a decision circuit decides if the reached value represents Node ID zero or one.

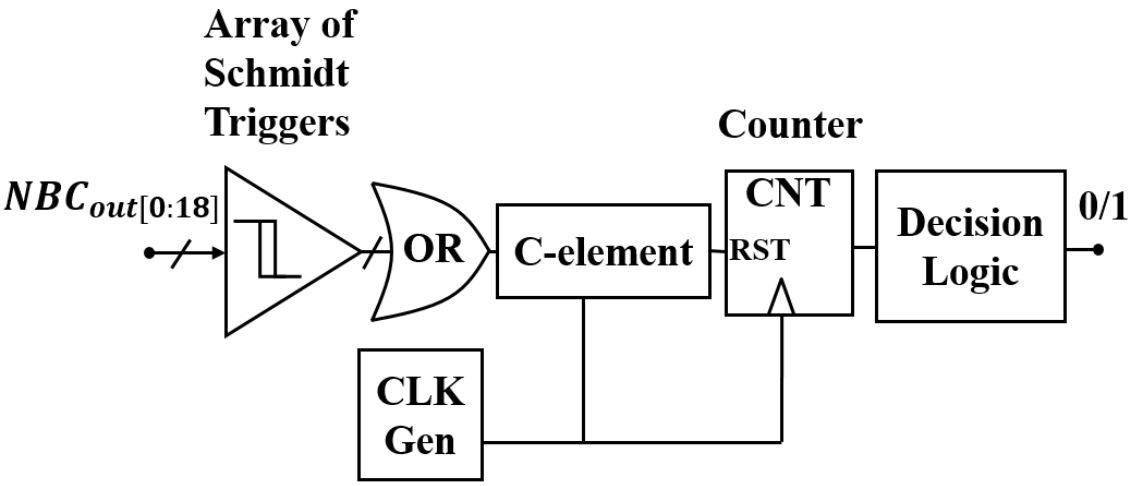


Figure 5.30: *Block diagram of the proposed digital processing*

Figure 5.31 shows the measured output of the NBC unit, where it is used to encode the transmitted node ID as a PPM scheme. The digital PPM signal is generated after the OR gate as shown in Figure 5.32. Figure 5.33 shows the output of the decision logic, which decodes the counter value and generates the transmitted node ID, so it can be compared with the WSN node fixed internal ID, and hence a wake-up signal is asserted or not.

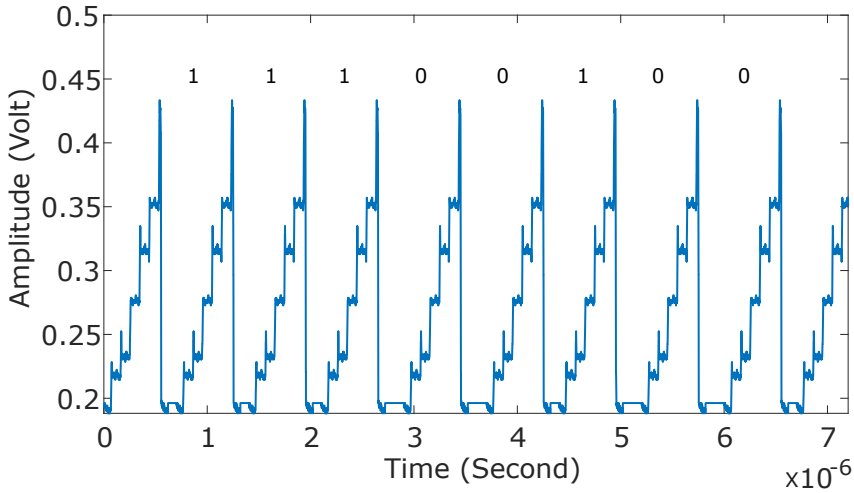


Figure 5.31: *NBC unit output encoding the transmitted node ID as a PPM scheme*

5.5 Benchmark

Table 5.1 shows the benchmark of the designed receiver compare to other low-power low data-rate receivers. The designed receiver exhibits a higher data-rate and a passive co-channel interference robustness provided by the SAW correlator. The receiver sensitivity

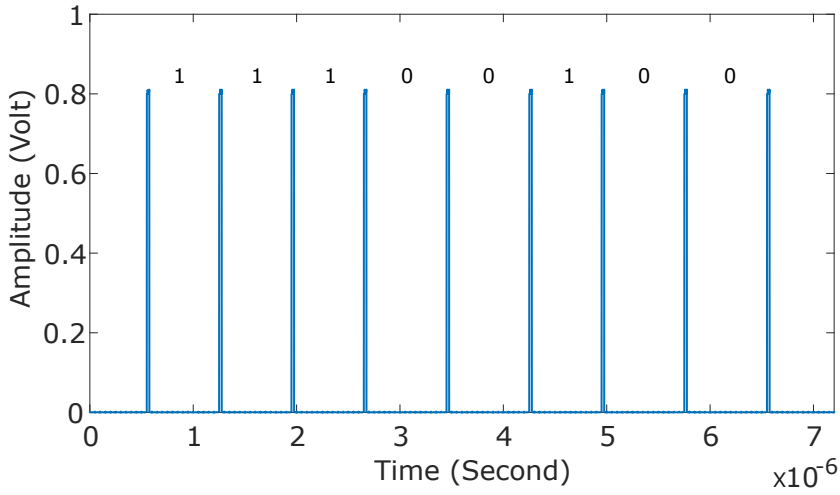


Figure 5.32: *Generated digital node ID as a PPM scheme*

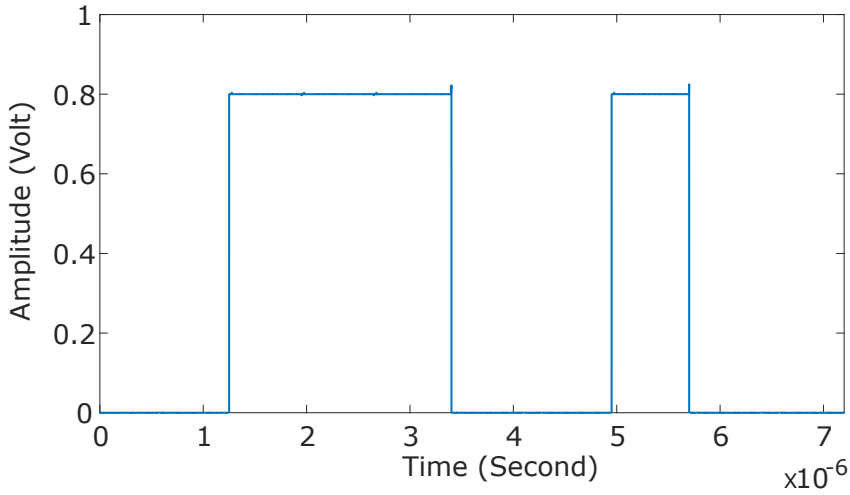


Figure 5.33: *Decoded PPM node ID*

can be further improved if the baseband amplifier gain is further increased. The relative high power dissipation comes from the high baseband bandwidth and the high gain baseband amplifier. The used modulation in the designed WuRx is based on OOK combined with PPM, where most of the other state-of-art receivers use OOK alone. From the chip area, the designed WuRx lies within the state-of-art areas.

Table 5.1: *Benchmark*

Reference	Frequency (GHz)	Sensitivity (dBm)	Data-rate (kbps)	Modulation scheme	Working Scheme	Power (μW)	Core Area (mm^2)	Process (nm)
[16]	2.4	−64	100	OOK	Always-on	51	0.36	90
[17]	2.4	−65	100	OOK	Always-on	10	0.42	180
[59]	2.4	−82	500	OOK	Duty-cycled	420	0.20	65
[15]	2.0	−72	100	OOK	Always-on	52	0.10	180
[60]	2.0	−100.5	100	OOK	Always-on	400	1.00	130
[18]	1.9	−56	100	OOK	Always-on	65	0.16	90
[61]	0.915	−86	10	OOK	Always-on	123	4.00	90
[62]	0.9	−94	20	FSK	Always-on	1200	1.10	250
This work	**2.44**	**−50**	**600**	**OOK, PPM**	**Always-on**	**142**	**0.51**	**65**

6 Conclusion and Future Work

This dissertation presents the design, implementation and fabrication of a novel low-power low-data-rate receiver, which can be used in WSNs as a WuRx. The communication process in WSN consumes significant amount of power, which degrades significantly the network operating lifetime and communication reliability. If the base station coordinates the communication and a WuRx is added to every node, the communication becomes asynchronous, real-time and on-demand, which reduces the power dissipation significantly. The designed WuRx uses direct-detection radio architecture to allow for low-power dissipation. However, direct-detection receivers suffer from low-receiver sensitivity and do not provide any co-channel interference suppression, which leads to receiver desensitization and high probability of false alarms. Therefore, WuRx should not only be power-efficient but also robust to co-channel interference. Usually co-channel interference robustness is achieved by means of a heterodyne or homodyne receiver architecture and narrowband filtering, but that requires highly linear RF amplifiers and mixers as well as a local oscillator which leads to high power dissipation.

The designed WuRx uses 13-bits 2.44 GHz BPSK Barker-coded SAW correlator as a prior stage to the WuRx IC. The SAW correlator provides a passive mechanism for co-channel interference robustness, which makes it a suitable approach in low-power receiver design. The measured SAW correlator exhibits an amplitude compression gain of $5-6$ dB, which makes the amplitude gain equals to Av = 0.42, when 13-bits BPSK Barker-coded signal at 2.42 GHz (due to the SMP 20 MHz center frequency shift) is used as an excitation signal, while other in-band signals are subject to 12 dB of attenuation. The 13-bits Barker code is a relatively short code, which achieves a compact device size of 3 mm^2. Longer code sequences could be used, to achieve better co-channel interference robustness. However, it comes at the expenses of larger correlator size and IL. A direct-detection receiver PCB with discrete devices is designed and fabricated to verify the concept of co-channel interference robustness provided by the SAW correlator. The measurements shows that the use of 13-bits BPSK Barker-coded excitation signal is 5-6 dB larger, when compared with the detected and amplified WiFi or sine wave signal at 2.42 GHz.

The WuRx IC is designed and fabricated in CMOS TSMC65n technology. The direct-detection circuit is based on active RF envelope detector that is biased in sub-threshold region, which is suitable operating region for low-power receiver applications. The active RF envelope detector allows also for impeded impedance matching. Due to the small RF pulse width, the direct-detection receiver has a large baseband bandwidth, which reduces both the front-end and the baseband sensitivity. However, the sensitivity is improved by reducing the baseband bandwidth. The innovative concept of the NBC in conjunction with PPM allows for scalable improvement of the total receiver sensitivity, at the cost of reduction in the communication data-rate. The maximum receiver sensitivity that is achieved is -50 dBm at a data-rate of 600 kbps. A sensitivity enhancement can be achieved if design factors are improved such as the SAW correlator IL, the RF envelope detector noise floor, in addition to larger gain in the baseband amplifier. The WuRx IC dissipates 142 μW from 1.2 V supply voltage without duty-cycling. The baseband amplifier occupies most of the power budget due to its high gain and wide amplification bandwidth. The WuRx chip

core area is 0.51 mm^2, which complies with the receiver IC targeted size.

From the WuRx application perspective, using a 1.2 V 4000 mAh battery, is sufficient to power-up the WuRx for more than three years given that the always-on power dissipation is 142 µW. The WuRx internal node ID register can be designed with 10-bits, allowing to have a WSN with 2^{10}. If the node ID uses 10-bits, the wake-up signal can be asserted to the WSN to start communication in less than 17 µs, given that the data-rate is 600 kbps at a sensitivity of −50 dBm.

Future work could include better design of the SAW correlator that improves the compression gain, and hence provides better co-channel interference robustness, and to minimize the device power losses. On the WuRx chip side, reducing the noise factor of the RF envelope detector increases the front-end sensitivity. Reducing the baseband amplifier power dissipation is another corner of enhancement. Improving the baseband gain and making it variable improves the sensitivity scalability, however, the data-rate would decrease.

Publications by the Author

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This work demonstrates the design, implementations and measurements of a 2.44 GHz direct-detection Wake-up Receiver (WuRx) based on Surface Acoustic Wave (SAW) correlator. The choice of direct-detection architecture for Radio Frequency (RF) radios allows for low-power dissipation. However, it suffers from high sensitivity to co-channel interference and poor receiver sensitivity, which reduce the communication performance and reliability. To improve the receiver sensitivity, the baseband bandwidth is reduced by means of an innovative Narrowband Correlator (NBC) in conjunction with Pulse Position Modulation (PPM) communication scheme, which allows for scalable receiver sensitivity versus data-rate. Additionally, to improve co-channel interference robustness, the receiver architecture uses 2.44 GHz 13-bits Binary-phase Shift Keying (BPSK) Barker-coded SAW correlator, which is fabricated on Lithium Niobate ($LiNbO_3$) substrate. It functions as a passive detection stage to the input RF signal and provides a mechanism for interferer suppression. The receiver is designed in CMOS TSMC65nm technology and achieves a power dissipation of 142µW from a 1.2V supply source, and a receiver sensitivity of -44dBm and -50dBm at a data-rate of 2Mbps and 600kbps respectively.

The WuRx can be used in Wireless Sensor Networks (WSNs) to reduce the power dissipation of nodes and extend their operating lifetime. WSN nodes are often powered by batteries, which makes the power dissipation the major challenge in the design of WSN. If each WSN node contains an integrated WuRx, which is always-on and listening for a wake-up signal from other nodes or the base station, the communication scheme becomes asynchronous, real-time and on-demand. Additionally, the WuRx with improved co-channel interference robustness reduces false positive wake-up signals to the WSN nodes, and provides a reliable communication scheme for the WSN in coexistence with other wireless systems.