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Ultrabroadband Sampling Circuits in SiGe BiCMOS Technology for Time Interleaved Analog-to-Digital Converters

HEINZ NIXDORF INSTITUT
UNIVERSITÄT PADERBORN

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Ultrabroadband Sampling Circuits in SiGe BiCMOS Technology for Time Interleaved Analog-to-Digital Converter

Ultrabreitbandige Sampler in SiGe-BiCMOS-Technologie für Analog-Digital-Wandler mit zeitversetzter Abtastung

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Abstract

This work investigates ultra-broadband sampling techniques for time-interleaved analog-to-digital converters. The sampling techniques are mathematically analyzed in detail and compared with each other. The mathematical analysis allows to predict multiple sampler characteristics including sampler bandwidth, sampling precision and so on. Two different sampling techniques are studied. The conventional sampling technique is implemented with a track and hold amplifier (THA) using switched emitter follower sampling topology. As an alternative sampling technique the short-time-integration (STI) technique using an integrate-and-hold circuit (IHC) is implemented. Three samples chips (2 THA chips and 1 IHC chip) were fabricated in state-of-the-art 130 nm SiGe BiCMOS technology. The measured results exceed the state of the art in samplers wrt. bandwidth and effective resolution (effective number of bits, ENOB).

Zusammenfassung

Diese Arbeit untersucht Ultrabreitband-Abtasttechniken für zeitversetzte Analog-Digital-Wandler. Die Abtasttechniken werden mathematisch detailliert analysiert und miteinander verglichen. Die mathematische Analyse ermöglicht die Vorhersage mehrerer Sampler-Eigenschaften, einschließlich Sampler-Bandbreite, Sampling-Präzision usw. Zwei verschiedene Abtasttechniken werden untersucht. Die konventionelle Abtasttechnik wird mit einem Track-and-Hold-Verstärker (THA) unter Verwendung einer geschalteten Emitterfolger (SEF) Abtasttopologie implementiert. Als alternative Abtasttechnik wird die short-time-integration (STI) Abtasttechnik, die eine Integrier-und-Halteschaltung (integrate-and-hold circuit, IHC) benutzt, implementiert. Drei Sampler-Chips (2 THA-Chips und 1 IHC-Chip) werden in einer modernen 130 nm SiGe BiCMOS Technologie hergestellt. Die Messergebnisse übertreffen den Stand des Technik im Hinblick auf Bandbreite und effektive Auflösung (effective number of bits, ENOB).

Ultrabroadband Sampling Circuits in SiGe BiCMOS Technology for Time Interleaved Analog-to-Digital Converters

Contents

1 Introduction

1.1 Motivation

High-speed broadband analog-digital-converters (ADCs) are critical components in modern digital communication systems, high-end measurement equipment, and other accurate real-time applications, like medical imaging or radar detection. The performance of a high-speed broadband ADC is usually measured by means of several key specifications including sampling rate, bandwidth, effective resolution and so on. A lot of study and research aim to improve the ADC performance, in order to meet the requirements of emerging applications. In order to achieve ultra-broadband operation and high sampling rate, the interleaving technology is being used, which can be achieved either in the time domain or in the frequency domain, using the so called time-interleaved (TI) ADC and frequency-interleaved (FI) ADC architecture. These two interleaving topologies will be briefly introduced in this chapter. However, the main focus in this thesis is on the TI ADC, especially suitable samplers for TI ADCs.

1.1.1 TI ADC vs. FI ADC

A TI ADC has a multi-channel structure with several ADCs in parallel [1]. It is widely used when the single ADC is not fast enough. Figure 1-1 shows a basic structure of the TI ADC consisting of samplers, ADCs, and digital signal processing (DSP). It has N parallel channels, whereby each channel has one sampler and ADC. The analog input signal is sampled and digitized by clocks with different phases. Each channel has a sampling rate of f_s/N, yielding a total sampling rate of f_s. The digitized output signal from each channel is processed by the DSP to reconstruct the data and generate the final digital output. Such structure uses DSP instead of multiplexer for data reconstruction, which is very common nowadays for ultra-high-speed TI-ADC system [2].

An FI ADC shown in Figure 1-2(a) using hybrid filter bank to overcome the channel mismatch in TI ADC was proposed [3]. The idea of FI is to do the data acquisition for different frequency bands in a multi-channel approach. The hybrid filter bank means the analog filter H_N before each sub-ADC for frequency band selection, and the digital filter F_N after the sub-ADC for reconstruction. Figure 1-2(b) shows an alternative structure of FI ADC which is more widely used [4]. This N channel FI structure uses down-conversion mixers and low-pass filter (LPF) in each channel to shift the specific frequency band to the base-band. Since the actual analog input signal before the sub-ADC is frequency limited, it relaxes the sampling rate in each channel, thus increasing the overall sampling rate. The digitized signals after the sub-ADCs are reconstructed in the DSP.

Analyzing single channel of TI and FI, it is easy to discover that the difference of their working principles are that TI uses direct-sampling while FI uses mix-and-sampling. The structure of FI shows its potential on increasing the bandwidth, but its jitter benefit compared to TI can be annihilated by the phase noise during the mixing process [5]. Both TI and FI have their pros and cons. Whether to choose TI or FI architecture depends on

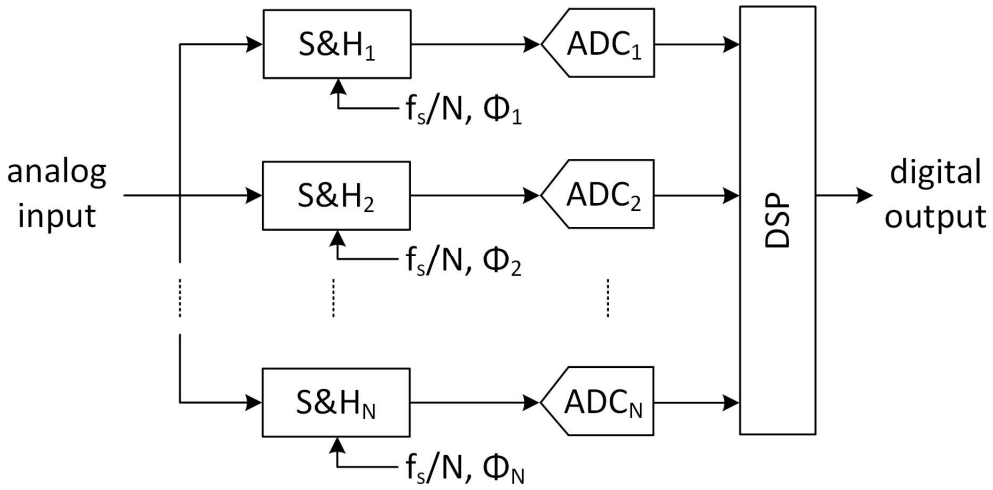


Figure 1-1: *Basic structure of the TI ADC*

the bandwidth and sampling rate of the application and the speed of the transistors in the selected semiconductor technology. In addtion due to somewhat unprecise pre-processing in the FI ADC, the post-processing in the DSP is more complex and power hungry. Therefore the TI ADC is a popular methodology in many applications. In this thesis, the main focus will be on the TI topology.

TI and FI ADCs have both shown their potential for the high-end real-time oscilloscopes. Keysight offers an oscilloscope with 110 GHz bandwidth and 256 GS/s sampling rate using 4 channel TI technology, while the effective number of bit (ENOB) range is from 6.8 bits to 5.0 bits [6]. The oscilloscope from Teledyne LeCroy is able to achieve 100 GHz bandwidth and 240 GS/s sampling rate with 2-channel FI technology [7].

1.1.2 Challenges in TI ADC Design

One of the main design challenges of this structure is the effect of mismatches, including offset, gain, and timing mismatches. These effects are analyzed and the correction and calibration method are discussed in [8].

Clock jitter is a major issue for high-speed ADCs. Above a certain input signal frequency, the ENOB is no longer limited by the thermal noise or the distortion, but the aperture error caused by the jittery sampling clock [9]. One solution to this issue is to use photonic sampling with an MLL as clock source, or a photonic PLL with an MLL as reference [10]. [11][12] shows a PLL with MZM (Mach-Zehnder modulator) based phase detection. It achieves a jitter of less than 4 fs integrated rms jitter from 5 to 20 GHz.

TI ADC is able to maximize the sampling rate by multi-channel topology, however the bandwidth is limited by the sampler of each single channel. State-of-the-art ultra-broadband ADCs in CMOS technology are based on TI topology and use large numbers of low-power, low-speed sub-ADCs in parallel. Very high sampling rates approaching 100 GS/s and moderate power dissipation have been achieved and reported. The TI ADC presented in [13] uses 64 sub-ADCs and achieves a conversion rate of 90 GS/s with an analog bandwidth of around 20 GHz. Due to 32 nm SOI CMOS technology and the use of

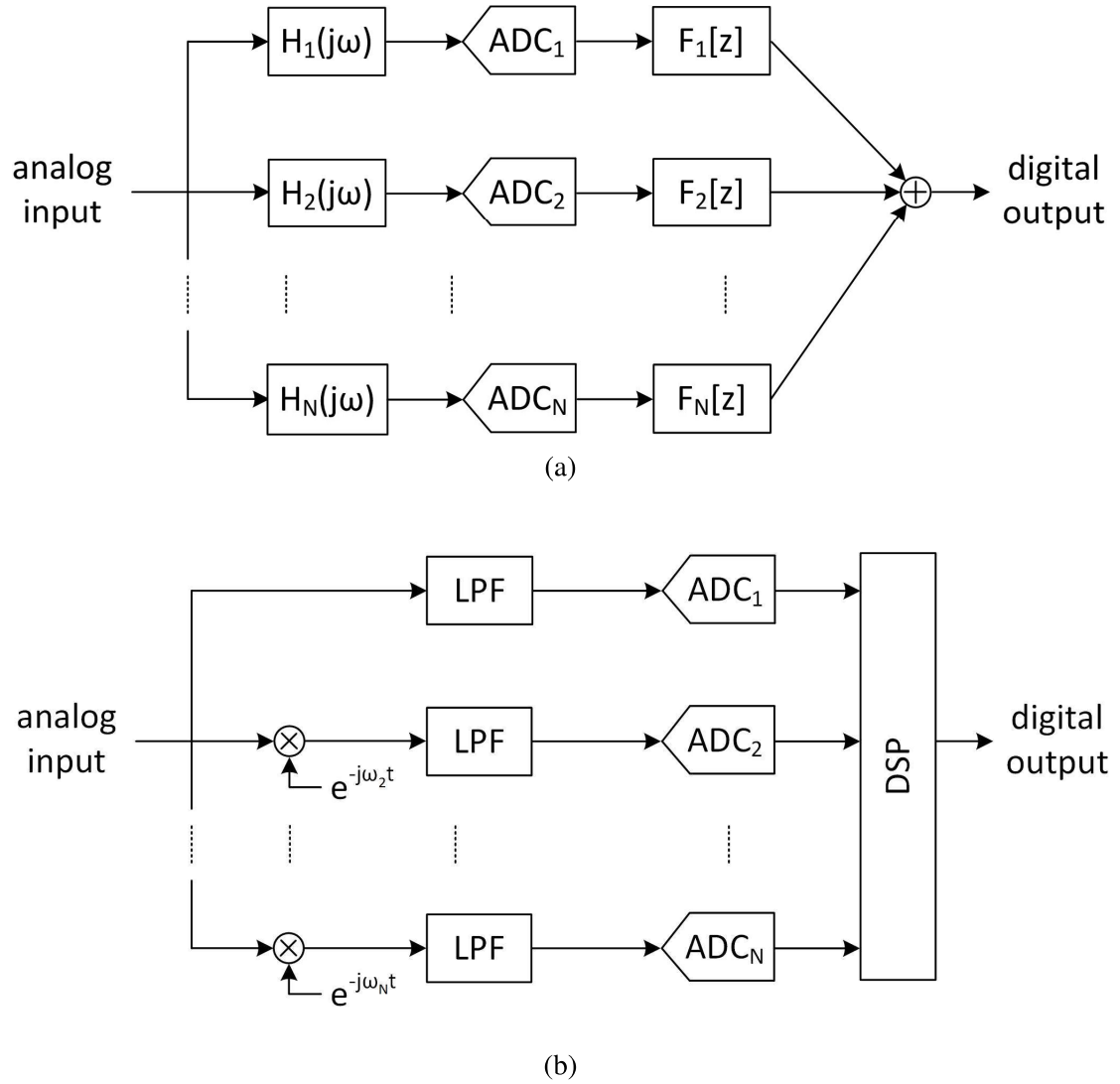


Figure 1-2: *Basic structure of the FI ADC, (a) original structure (b) alternative structure*

power-efficient successive-approximation sub-ADCs, it dissipates only 667 mW. A disadvantage of CMOS TI ADCs with high sampling rates is the limited bandwidth of the time-interleaved sampler. [14] reported the highest sampling rate single-chip TI ADC of 128 GS/s and 60 GHz input bandwidth in 22 nm Si/SiGe FDSOI CMOS technology. This chip uses 4 master and 32 slave track-and-hold amplifiers (THA) built with CMOS series switches.

In order to overcome the bandwidth bottleneck of TI ADC, this thesis will study and research on different ultra-broadband sampling technologies.

1.2 Outline of the Thesis

This thesis is organized as follows. In Chapter 2, sampling circuit fundamentals will be discussed, including different sampling technologies, sampler characteristics, measurement techniques for samplers, and the state-of-the-art in the ultra-broadband sampling

circuits. In Chapter 3, the circuit design and measurement results of a switched emitter follower (SEF) based input-buffer-less THA are presented. The work was published in [A1]. Chapter 4 introduces the design of a SEF based THA with buffer and its measurement results. The chip was published in [A2]. In Chapter 5, an STI IHC is presented with its principle and architecture, including the circuit diagram and measurement results. The chip was published in [A3], while the detailed theoretical analysis will be published in [A4]. This topology was also patented [A5]. Conclusions with the comparison of all the design to the state-of-the-art and an outlook are given in Chapter 6.

2 Sampling Circuit Fundamentals

In this chapter, commonly used sampling circuits are introduced, they are categorized as track-and-hold (TH) and charge sampling technologies, which are also referred to voltage-mode or current-mode sampler respectively. [15] gives an overview of the TH sampling technology, [16] introduces the idea of charge sampling technology. Different sampler characteristics are discussed including bandwidth, jitter, noise and so on. The state-of-the-art in ultra-broadband sampler are given at the end.

2.1 TH Sampling Technology

2.1.1 Principle of TH Sampling

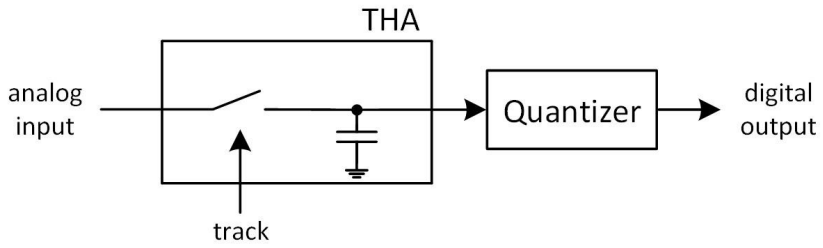


Figure 2-1: *Block diagram of an ADC built from TH sampler with quantizer*

The principle of an ADC using TH sampling is depicted in Figure 2-1. The track-and-hold amplifier (THA) samples the signal and the quantizer performs the analog-to-digital conversion. The THA is modeled with a switch controlled by the track signal and a hold capacitor. Figure 2-2 shows how the track signal is applied to perform the sampling function. The dashed line represents the input signal and the solid line is the output signal of the THA. The output signal exhibits two phases, track and hold phase. The hold signal is the sampled value at the end of the track signal. The concept of sample-and-hold amplifier (SHA) is actually two samplers connected with each other, the second sampler samples again the hold signal of the first sampler with inverted sampling clock.

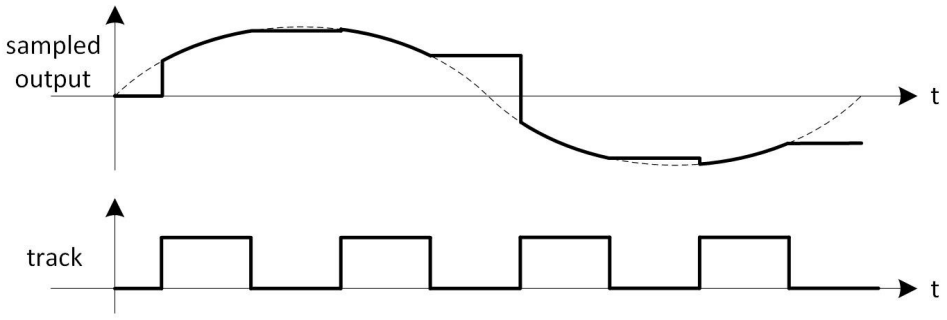


Figure 2-2: *Sampled signal and control signal of THA*

2.1.2 TH Sampling Topology

Switched-Capacitor Sampler

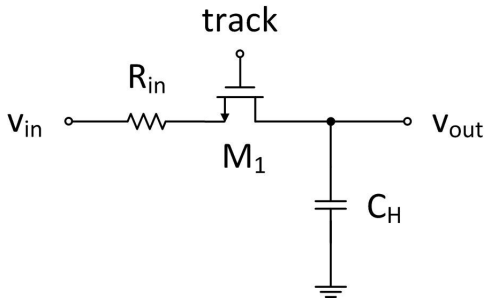


Figure 2-3: *Circuit diagram of switched-capacitor*

Switched-capacitor sampler is a sampling topology often used in CMOS technology. Figure 2-3 shows the circuit diagram of a switched-capacitor sampler [17]. The idea is to use MOS transistor M_1 as a transmission gate. R_{in} is the input resistance, C_H is the hold capacitor. When *track* is on, the circuit is in the track mode, v_{out} is equal to v_{in}. When *track* is off, it is in the hold mode, v_{out} is constant and equal to the stored value in C_H. Basically this is the most simplest structure for a sampler.

Diode-Bridge Sampler

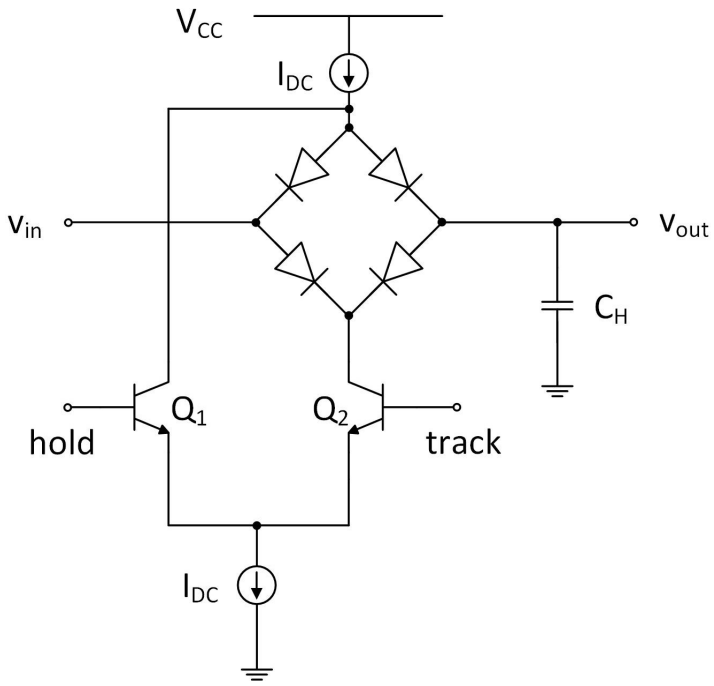


Figure 2-4: *Circuit diagram of diode-bridge*

The diode-bridge sampler is a traditional way to implement the sampling function in analog design [18]. Figure 2-4 shows a basic implementation of the diode-bridge THA. In

the track phase, Q_2 is on, the DC current I_{DC} flows through the diode-bridge. The output v_{out} follows the input signal v_{in}, the expression of v_{out} is shown below.

$$v_{out} = v_{in} - I_{B3,ON}R_{in} - V_{BIAS,ON} \tag{2-1}$$

In the hold mode, the current flows through Q_1, therefore the diode-bridge is switched off, the output port is blocked from the input signal. The impedance of the diode in the small-signal analysis during the track mode is $1/g_m$ and small, which allows to achieve large bandwidth.

Switched-Emitter-Follower Sampler

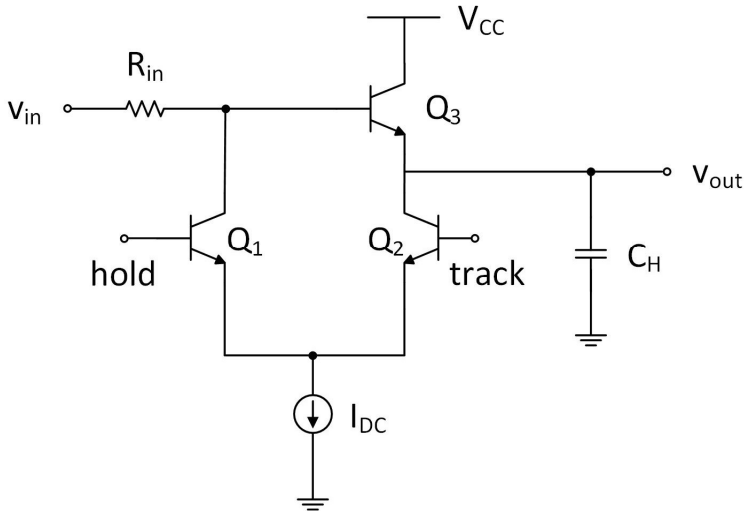


Figure 2-5: *Circuit diagram of SEF*

The switched-emitter-follower (SEF) sampler is the most popular sampler topology used in bipolar technology. The circuit diagram is shown in Figure 2-5 [19]. In this structure, transistor Q_3 works as the emitter follower while $Q_{1,2}$ control the DC current through the emitter follower. In the track mode, Q_2 is on, the emitter follower drives the hold capacitor C_H, v_{out} is equal to $v_{in} - V_{BE3,on}$. In the hold mode, Q_1 is on, the DC current through the input resistor R_{in} reduces the base voltage of Q_3, and Q_2 is off to set emitter current to zero. These switches the emitter follower off so that v_{out} keeps the stored value in hold capacitor C_H.

2.2 Charge Sampling Technology

Charge sampling using an integrate-and-hold circuit (IHC) is another possible sampling technique. In a charge sampler the input waveform is integrated over a fixed time window (e.g. the period of a digital clock signal or a local oscillator signal of a radio frequency receiver) and the integration result is taken as the sample [20][21]. Most charge sampler for electrical signals so far focus on the implementation of tunable filters and their

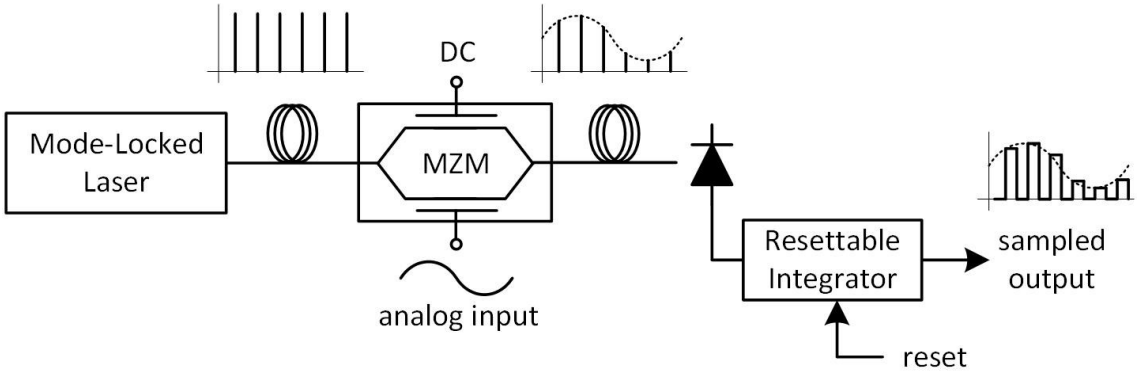


Figure 2-6: *Block diagram of a photonic sampler using mode-locked laser and MZM.*

circuit implementations are not suited for ultra-broadband samplers [22][23][24]. Charge sampling is also used in photonic samplers using an MLL as optical clock [10][11][12].

The principle of this type of optic sampling is shown in Figure 2-6. A sequence of ultra-short optical pulses is generated by means a of mode-locked laser (MLL). The amplitude of the electrical input signal is modulated onto the optical pulses using an MZM (Mach-Zehnder-Modulator). Hence the optical output signal of the MZM represents a sequence of dirac-like pulses which are weighted by the amplitude of the electrical input signal. Subsequently in a photo detector the modulated optical pulse sequence is converted to a current pulse sequence which is fed to the input of a resettable integrator. Before each integration of an amplitude-weighted current pulse the integrator is reset. Then the integrator integrates the pulse and when the pulse has decayed it provides a constant voltage, the hold signal. In this way the integrator acts as an IHC. Each hold signal is proportional to the current-time-product rsp. charge of a weighted current pulse rsp. the instantaneous voltage of the electrical input signal of the electro-optic modulator.

It should be noted that the optical pulses exhibit a certain pulsewidth in the range of a few picoseconds or femtoseconds [25]. Hence, strictly speaking, the output signal of the photonic sampler is not proportional to the *instantaneous* electrical input signal but rather to a *short-time integral* of the electrical input signal. Hence in the following this type of sampling will be called short-time integrate (STI) sampling. The STI sampling concept can also be implemented using all-electronic circuits.

2.2.1 Principle of Charge Sampling

In Figure 2-7 the concept of the charge sampler based on an IHC and quantizer is shown. The IHC comprises two components, a switch to control track and hold periods and a resettable integrator which performs the integration and the reset. The IHC has two control signals, track and integrate, which represent digital signals controlling the operation of the switch and the integrator. The track signal determines when and how long the analog input signal should be passed to the integrator. When the track time is extreme short, it realize the STI sampling. The integrate signal controls the integrate (integrate=1) and reset phase (integrate=0) of the integrator. The track and integrate signal must be synchronized to each other.

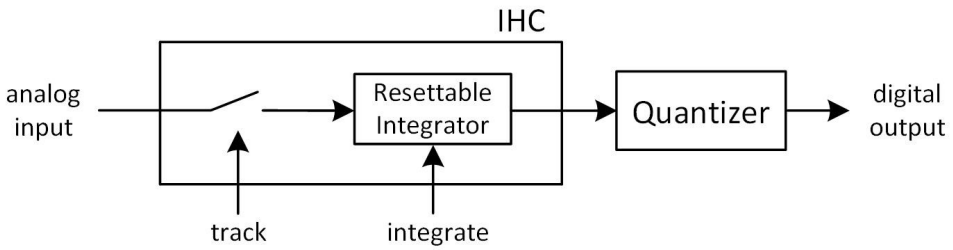


Figure 2-7: *Block diagram of an ADC built from charge sampler with quantizer*

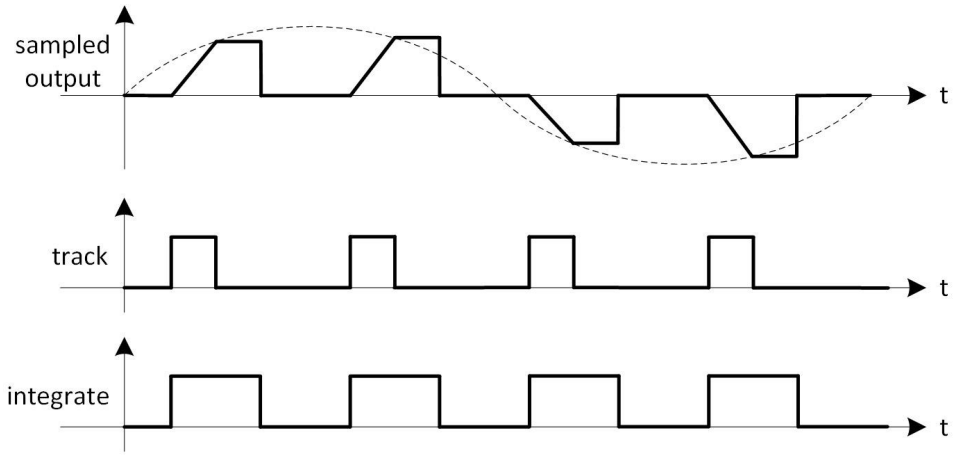


Figure 2-8: *Sampled signal and control signals of IHC*

Figure 2-8 shows how track and integrate signals can be used to perform the integrate and hold (IH) function. In the first plot, the dashed line represents the input signal and the solid line the output signal of the IHC. The output signal exhibits three phases: integrate, hold and reset phase. When the signal is tracked during the integration phase (track=integrate=1), the integrator integrates the input signal. When the signal is not tracked while the integrator is still in the integration mode (track=0; integrate=1), the integrator will integrate a zero input and act as a hold circuit. When the integrator is reset (integrate=0) the output of the IHC will be reset. The frequencies of the track and integrate signals are equal but their phases are different and have to be carefully adapted. Table 2-1 shows the control signals and the corresponding states of the IHC.

Table 2-1: *Control signals and states of IHC*

IHC Control Signals		IHC States
track	integrate	
0	0	reset
0	1	hold
1	0	reset
1	1	integrate

The hold signal of the IHC does not represent the instantaneously sampled input signal

but the average of the input signal during the integration period, i.e. the IHC performs STI sampling. However, if the pulse width of the track signal is made very short and the integrator gain is large enough, the average values can be considered as quasi-instantaneously sampled values. Hence for short track pulses the STI sampler operates in a similar way as a THA. Actually it is shown in the following that the duration of the integrate state determines the frequency response and bandwidth of the IHC in a very similar way as the RC time constant of a resistive switch and a hold capacitor determines the frequency response and bandwidth of a conventional THA.

2.2.2 Charge Sampling Topology

Photonic Sampler

When the charge sampling is used in a photonic ADC, the input charge is absorbed by the photodiode to generate the current pulse as input signal. Figure 2-9 shows the circuit diagram of a photonic sampler using charge sampling [26]. The photons are absorbed by diode D_1, the current pulse is transferred to voltage through resistor R_D. Q_3 and C_{INT} construct a GmC integrator. This topology has only two states, integrate and reset, controlled by clock signal *int* and *res*. The duration of the current pulse is much shorter than the clock duration, when the pulse is over, the rest time of the clock duration will integrate zero input, which shows the effect of a hold signal. When *int* is on, v_{out} is the integrated signal based on the DC level of *int*. When *res* is on, v_{out} is set to be a fixed DC level through Q_2. The sampled value at the output is the integration of a pulse, it can be understood as the energy of the pulse.

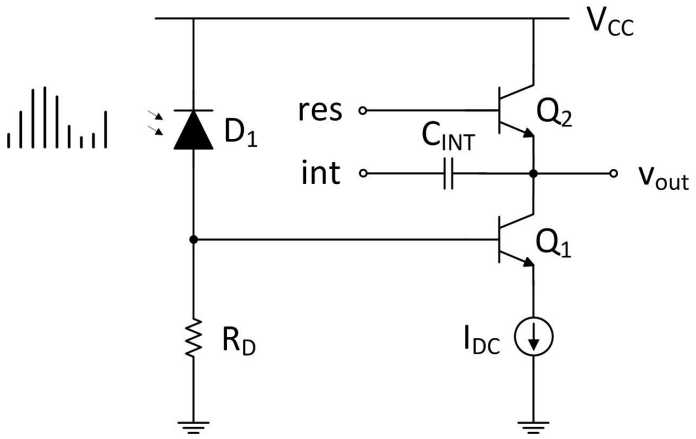


Figure 2-9: *Circuit diagram of photonic sampler*

STI Sampler

STI sampler realizes an ultra-broadband charge sampler with general analog input signal instead of optical pulse signal. In order to manually generate the pulse, an extra clock state of hold is introduced compared to photonic charge sampling. Figure 2-10 shows the circuit diagram of an STI sampler [27]. The input current source i_{in} works as tail current

of differential transistor pair $Q_{1,2}$. Q_2 and C_{INT} construct a GmC integrator. When *int* is on, the instantaneous output value of v_{out} is the integration of i_{in} over the duration of *int*. When *hold* is on, the input current is shifted from Q_2 to Q_1. Mathematically the sampled value of this sampling method is the average input signal over the duration of *int* signal.

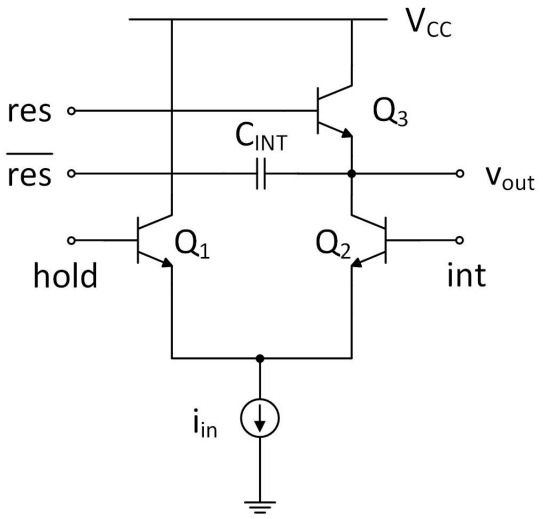


Figure 2-10: *Circuit diagram of STI sampler*

2.3 Comparison of TH and Charge Sampler Characteristics

As the front-end of a whole ADC system, the characteristics of the sampler typically dominate the performance of the ADC. This section introduces several core characteristics for the ADC sampling and compares them between TH and charge sampler.

2.3.1 Bandwidth

The bandwidth is the most concerned issue for TI ADC. For a sampling system, the bandwidth for large-signal and small-signal is different. The large-signal bandwidth means the bandwidth of the sampled signal, which can be differed from the small-signal bandwidth.

The bandwidths of a THA and an IHC sampler can be analyzed from the simplified models as shown in Figure 2-1 and 2-7, respectively. The model of TH in Figure 2-1 is constructed by a switch and a hold capacitor C_H. The small-signal bandwidth is defined when the TH circuit is in the track mode, which means the switch is on. Therefore the equivalent circuit is an RC low-pass filter with switch on resistance R_{on} and C_H. The 3dB small-signal bandwidth of a TH sampler in track mode is calculated in Equation (2-2). However the large-signal bandwidth is highly depending on the transition speed of the switching process between track and hold mode.

$$f_{3dB} = \frac{1}{2\pi R_{on} C_H} \tag{2-2}$$

The IHC model in Figure 2-7 consists of a switch and a resettable integrator. According to Table 2-1, the sampling is done during the integrate state. If the duration of the integrate state is short, STI sampling is achieved. The duration of when *integrate* = *track* = 1 is represented by T_i. Signal processed by the IH is expressed in Equation (2-3),

$$v_o(t + T_i) = A_i \int_t^{t+T_i} v_{in}(\tau)\, d\tau = \frac{1}{T_i} \int_t^{t+T_i} v_{in}(\tau)\, d\tau \tag{2-3}$$

where $v_o(t + T_i)$ is the signal in the hold mode, $v_{in}(t)$ is the input signal and T_i is the duration of the integrate state. A_i is the DC gain of the integrator. In order to obtain the average of $v_{in}(t)$, A_i is chosen to be $\frac{1}{T_i}$. Mathematically this average process can be modeled by subtracting the integration from 0 to t by the result from 0 to $t - T_i$, yields

$$v_o(t) = \frac{1}{T_i} \int_0^t v_{in}(\tau)\, d\tau - \frac{1}{T_i} \int_0^{t-T_i} v_{in}(\tau)\, d\tau = \frac{1}{T_i} \int_{t-T_i}^t v_{in}(\tau)\, d\tau. \tag{2-4}$$

The transfer function of the IHC is given in Equation (2-5)

$$H_{IHC}(j\omega) = \frac{1}{T_i}\left(\frac{1}{j\omega} - \frac{1}{j\omega} \cdot e^{-j\omega T_i}\right). \tag{2-5}$$

The magnitude response of the IHC yields Equation (2-6)

$$|A_{IHC}(\omega)| = \frac{1}{T_i\omega} \sqrt{2 - 2\cos(\omega T_i)} = \frac{\sin(\omega \frac{T_i}{2})}{\omega \frac{T_i}{2}}. \tag{2-6}$$

Rewriting the magnitude response using input frequency f_{in} and integration duration T_i as parameters, yields

$$|A_{IHC}(f_{in}, T_i)| = \frac{\sin(\pi f_{in} T_i)}{\pi f_{in} T_i}. \tag{2-7}$$

Therefore, the frequency response of STI sampling is a *sinc* function where both gain and bandwidth depend on T_i. The 1dB and 3dB bandwidth can be calculated to

$$f_{1dB} = \frac{0.261}{T_i} \qquad f_{3dB} = \frac{0.442}{T_i} \tag{2-8}$$

This means that if the input frequency is smaller than f_{3dB}, the IHC operates approximately as a bandwidth-limited instantaneous sampler. Intuitively this can be understood from that the average value of the signal during an extreme small period is an instantaneous value. The IHC designed to work for the frequency up to f_{3dB} is an STI sampler.

Table 2-2 shows different integration durations T_i of the IH and the corresponding bandwidths and DC gains. Assume that the STI IHC has tunable T_i, reducing T_i will also reduce the DC gain. If the IHC is designed for unity gain with 10 ps, 5 ps as half of the original T_i results in half DC gain.

Figure 2-11(a) shows different frequency responses of the IHC with T_i as parameter and DC gain normalized to 1. The frequency response has the shape of a *sinc* function. The dashed lines represent the gain equal to 0.891 (-1dB) and 0.708 (-3dB), respectively. The characteristic lines from left to right use different integrate duration values as 10 ps, 7

Table 2-2: *STI IHC with different average duration*

T_i	f_{1dB}	f_{3dB}	$Gain_{dc}$
10 ps	26.1 GHz	44.2 GHz	0 dB
7 ps	37.2 GHz	63.1 GHz	-3.1 dB
5 ps	52.2 GHz	88.4 GHz	-6 dB

ps and 5 ps. The cross-points with the dashed lines represent different bandwidths. The bandwidth increases as the integrate duration reduces. Figure 2-11(b) shows different DC gain of IH when A_i is designed for 10 ps.

Figure 2-12(a) shows that both SH and charge samplers exhibit very similar amplitude response up to the 3dB cut-off frequency. Beyond the 3dB cut-off frequency the STI charge sampler exhibits a stronger roll-off and ripple. The phase response comparison in Figure 2-12(b) shows that the conventional SH sampler has better phase response performance because of flatter phase response near the 3dB cut-off frequency.

2.3.2 Sampling Jitter

Jitter analysis in a sampling system allows to predict voltage error due to time error. In the following, the voltage error in an STI sampler due to clock jitter is analyzed. Figure 2-13 shows how the time shift at a discrete sampling instant k leads to a voltage error on the signal $v(t)$, where $k = nT$ and T is the sampling period.

Similar as in jitter analysis of instantaneous sampling we use Equation (2-9) as the basis of jitter analysis whereby the error voltage is proportional to the derivative of the signal $v(t)$ when a jitter value $\delta_j(t)$ is on the sampling instant [28],

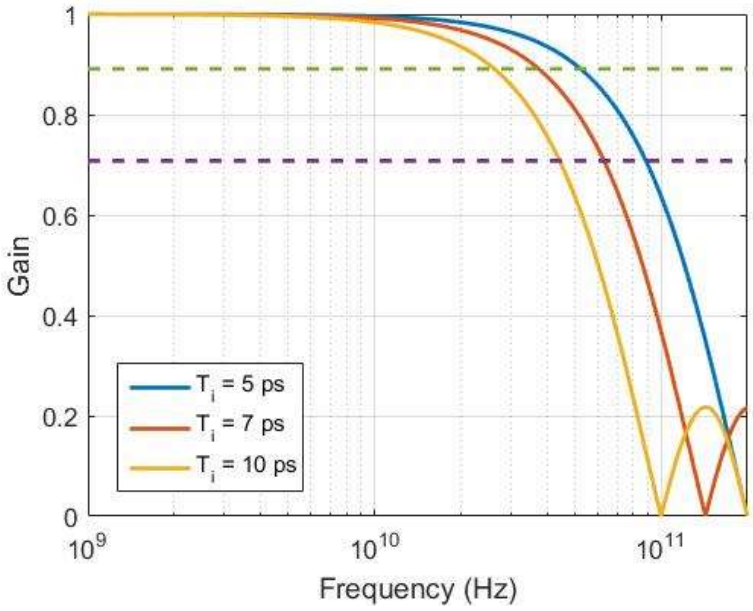
$$v_{err}(k) = \left.\frac{dv(t)}{dt}\right|_{t_{ideal}(k)} \cdot \delta_j(k) \tag{2-9}$$

with $\delta_j(k) = t_{ideal}(k) - t_{real}(k)$. Taking the root mean square (RMS) operation on the jitter error voltage, where $\sigma()$ is the root mean square operator, and δ_{j_rms} is the standard deviation (or RMS) of jitter, yields

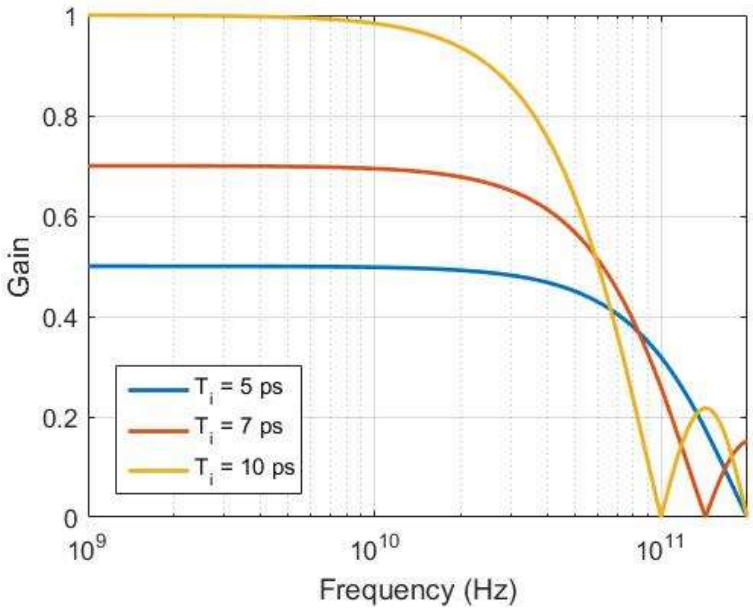
$$v_{err\_rms} = \sigma(v_{err}(k)) = \sigma\left(\frac{dv(t)}{dt}\right) \cdot \sigma_{j\_rms} \tag{2-10}$$

if $\left.\frac{dv(t)}{dt}\right|_{t_{ideal}(k)}$ and $\delta_j(k)$ are uncorrelated.

In the STI sampling system, the sampled value is the period average value. For the STI IHC, there is only one control signal and the duration of T_i is fixed. Therefore Equation (2-2) has only one parameter for jitter analysis, only the shift of the time window for the integration cause the voltage error, the integrate duration has no influence. The first order derivative used for the jitter analysis in the instantaneous sampling system can also be applied in the STI sampling system. Assuming the input signal is $A\sin(\omega_{in}t)$, the signal to be sampled is the period average of the input signal, based on Equation (2-2)(2-10),



(a)



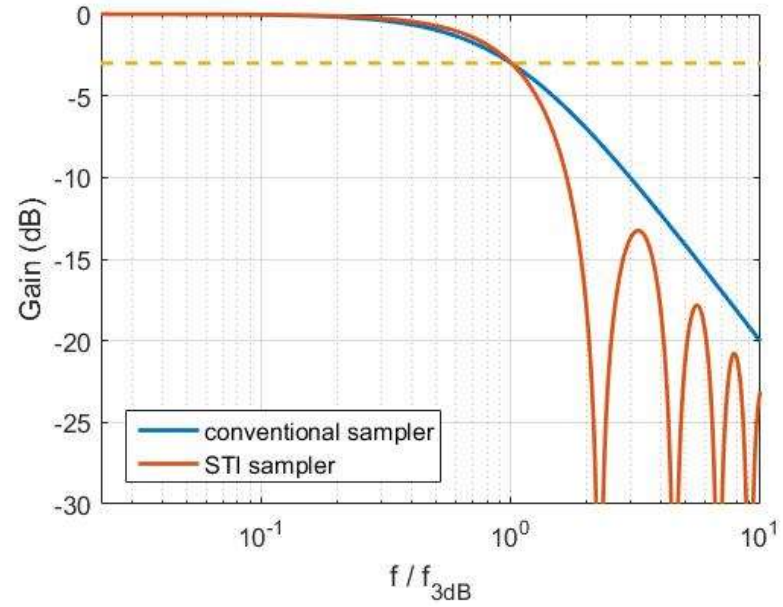
(b)

Figure 2-11: *(a) IH bandwidth with DC gain normalized to 1 (b) IH gain without normalized DC gain*

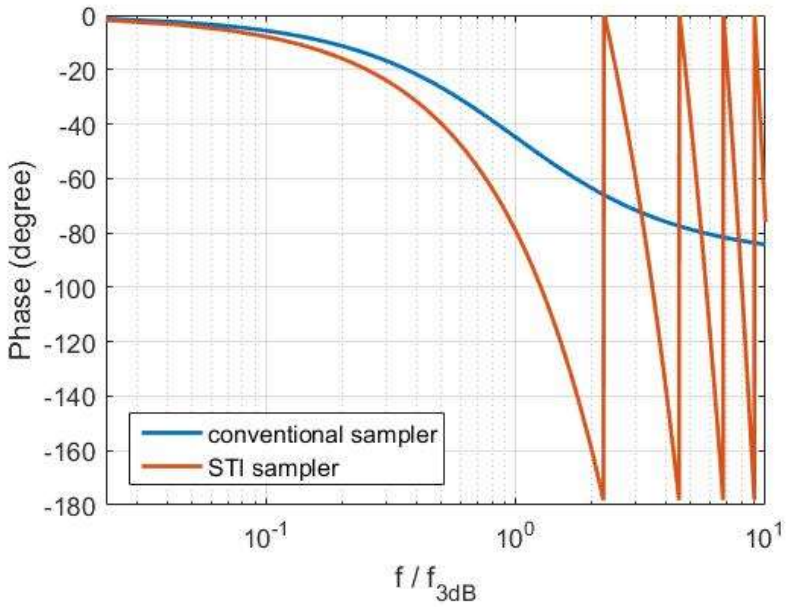
yields

$$v(t) = \frac{1}{T_i}\int_{t-T_i}^{t} A\sin(\omega_{in}t)dt = \frac{A\cos(\omega_{in}(t-T_i)) - A\cos(\omega_{in}t)}{\omega_{in}T_i}. \tag{2-11}$$

$$\begin{aligned}\frac{dv(t)}{dt} &= \frac{A}{\omega_{in}T_i}\Big(-\omega_{in}\sin(\omega_{in}t-\omega_{in}T_i)+\omega_{in}\sin(\omega_{in}t)\Big)\\ &= \frac{A}{T_i}\Big((1-\cos(\omega_{in}T_i))\sin(\omega_{in}t)+\sin(\omega_{in}T_i)\cos(\omega_{in}t)\Big).\end{aligned} \tag{2-12}$$



(a)



(b)

Figure 2-12: *Conventional SH sampler vs. STI charge sampler on (a) amplitude response (b) phase response.*

Taking RMS operation and assuming $\theta = \omega_{in}t$, yields

$$\sigma\left(\frac{dv(t)}{dt}\right) = \sqrt{\frac{1}{2\pi}\int_0^{2\pi}\left(\frac{dv(t)}{dt}\right)^2} = \frac{A}{T_i}\sqrt{\frac{(1-\cos(\omega_{in}T_i))^2 + \sin^2(\omega_{in}T_i)}{2}}. \tag{2-13}$$

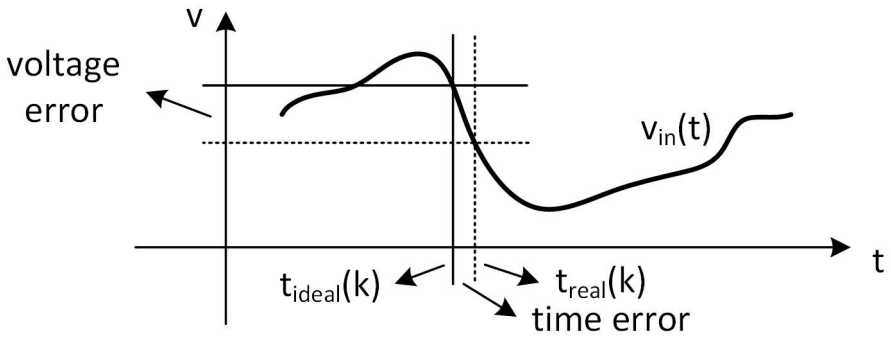


Figure 2-13: *time error vs. voltage error for the signal v(t)*

The RMS value of the voltage error in the average sampling system is given by

$$v_{err\_rms} = \frac{A\sqrt{1-\cos(\omega_{in}T_i)}}{T_i} \cdot \delta_{j\_rms}. \tag{2-14}$$

The signal to noise ratio (SNR) for sine wave as input signal and jitter noise is given by

$$SNR_{dB} = 20\log\left(\frac{\frac{A}{\sqrt{2}} \cdot \frac{1}{T_i\omega_{in}}\sqrt{2-2\cos(\omega_{in}T_i)}}{\frac{A\sqrt{1-\cos(\omega_{in}T_i)}}{T_i} \cdot \delta_{j\_rms}}\right) = -20\log\left(\omega_{in} \cdot \delta_{j\_rms}\right). \tag{2-15}$$

where the signal power is calculated based on the amplitude response of charge sampler. In the instantaneous sampling system, SNR degradation due to jitter has exactly the same expression [9]. Therefore the jitter performance of the STI sampler is the same as the jitter performance of instantaneous sampling.

2.3.3 Noise

The thermal noise analysis in the THA circuit uses the low-pass filter model. The noise power is depending only on the hold capacitor, yields kT/C, where k is the Boltzmann constant and T is the absolute temperature (in Kelvin) [9]. The thermal noise behaves differently on the integrator. To simplify the analysis, the ideal RC integrator is used as shown in Figure 2-14(a). Figure 2-14(b) applies the thermal noise as input noise. The transfer function of the simplified RC integrator model is as follows, it should not be the *sinc* function because the pulse generation is from the clock, the noise is generated from the integrator itself during the integration.

$$v_{out}(s) = |-\frac{1}{sRC}| \cdot v_{in}(s). \tag{2-16}$$

The relationship between the T_i and RC are presented as follows,

$$\frac{1}{T_i} = |-\frac{1}{sRC}| = \frac{1}{2\pi RC}. \tag{2-17}$$

The thermal noise model is the same as in the track and hold circuit, the power spectral density of the noise yields,

$$v_n{}^2(\omega) = 4\mathrm{kT}R. \tag{2-18}$$

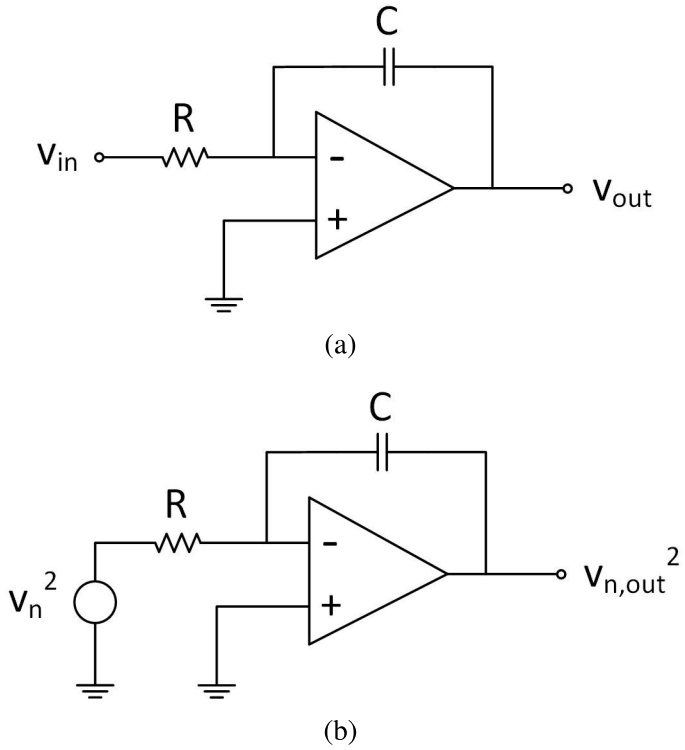


Figure 2-14: *(a) RC integrator model with ideal operational amplifier. (b) Noise equivalent circuit*

The noise power at the output is the integration of the output noise from 0 to T_0, where T_0 is the integration duration. It is equivalent to the integration from f_0 to ∞ in the frequency domain with $f_0 = 1/T_0$. In this system, T_0 is half of the sampling period because of the reset phase, thus $f_0 = 2f_s$. The result is shown in Equation (2-20).

$$v_{n,out}(f) = \frac{kT}{\pi^2 RC^2 f^2} \tag{2-19}$$

$$P_{n,out} = \int_{f_0}^{\infty} v_{n,out}(f)df = \frac{kT}{\pi^2 RC^2 2f_s} = \frac{kT}{C}\frac{T_i + t_{hold}}{\pi^2 T_i} \tag{2-20}$$

This result shows that the noise power of the thermal noise with the IHC is not only affected by integration capacitance and temperature but also by integration and hold time. The capacitor of IHC can be selected larger compared to the THA because it is not related to the bandwidth performance. Although the sampling rate is determined mainly by the conversion speed of ADC, a large integrator capacitor will also increase the reset time and thus decrease the clock frequency of the IHC. If we assume a fixed target bandwidth $BW(Ti)$, the hold time should be made as small as possible and integrator capacitor as large as possible without increasing reset time too much in order to achieve sufficiently high sampling rate.

2.3.4 Droop

The hold phase of a conventional THA and an STI sampler or IHC is fundamentally different. The conventional THA can be understood as a low-pass filter, the droop during the hold mode is the same as the RC natural response. The voltage droop is given by

$$v_{droop}(t) = v_0 - v_0 e^{-\frac{t}{R_{leak}C_{hold}}}, \tag{2-21}$$

where v_0 is the sampled voltage value, C_{hold} is the hold capacitor, R_{leak} is the leakage resistance during the hold mode. When the hold time is fixed, the larger $R_{leak}C_{hold}$ is, the less is the droop of the THA. However the bandwidth of the THA as a low-pass filter is $1/R_{switch}C_{hold}$, where R_{switch} represents the resistance of the sampling switch. For broadband THAs the hold capacitor is typically made small in the range of 50 fF. This however increases the droop. Thus the size of the hold capacitor is a trade-off between the droop and the bandwidth. Furthermore, thermal noise in the conventional sampler is proportional to $1/C_{hold}$.

For the STI sampler, the bandwidth is determined solely by the pulse width of the sampling pulse if the integrator is fast enough and does not depend on the integration capacitor. Hence in an STI sampler bandwidth can be optimized independently from droop and thermal noise. This is a major advantage of the STI sampler compared to conventional THAs.

2.4 Measurement Techniques for Samplers

The measurement of the samplers is done in both frequency domain and time domain. The frequency domain measurement is accomplished by S-parameter measurement, hereby testing the small-signal performance of the chip. The time domain measurement testing large-signal performance includes spectrum and transient measurements. The spectrum measurement is used to understand the dynamic and nonlinear performance of the sampler to obtain ENOB, SINAD, THD and so on. The transient measurement shows signal integrity issues for different input frequencies.

2.4.1 Small-Signal Measurement

S-parameters are measured with a broadband vector network analyzer (VNA). The measurement tests the small signal performance in track and hold mode separately. The differential input and output ports are connected with input and output ports of VNA respectively. If single-ended measurement is applied, one of the differential input and output ports is terminated with a 50 Ω resistor on chip and disconnected from the VNA. The chip is set either in track mode or hold mode using a static clock signal. Figure 2-15 shows the test setup for S-parameter measurement. The VNA enables four or two ports to test the chip under the differential or single-ended mode, a DC source is used to set the static clock state. S_{21} in track mode shows the small-signal bandwidth of the DUT while S_{21} in hold mode represent the signal feedthrough.

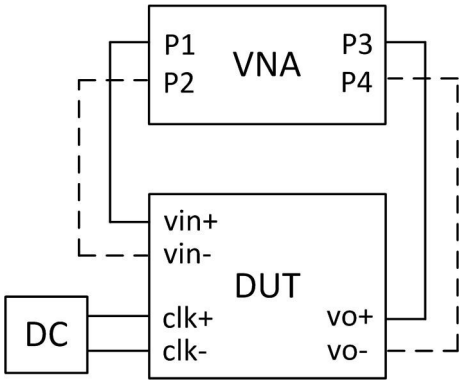


Figure 2-15: *Test setup for S-parameter measurement*

2.4.2 Large-Signal Measurement

Transient Measurement

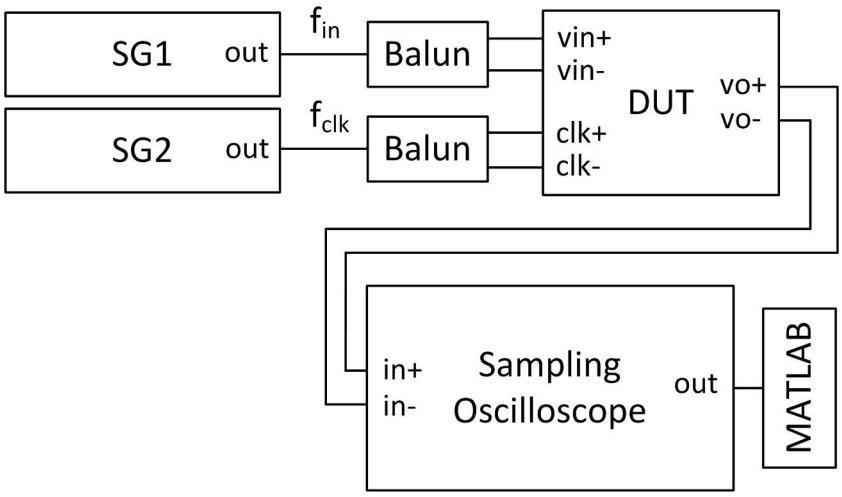


Figure 2-16: *Simplified test setup for transient measurement*

Figure 2-16 shows the test setup for transient measurement. SG1 is used to generate the input signaL, SG2 generates the clock. The sampling oscilloscope digitizes the output of the DUT. The differential output of the sampling oscilloscope is calculated off-line in MATLAB. For high frequency sampler measurement, the jitter between the signal and clock sources is a major issue, it is advised to synchronize the two signal sources together. Also the synchronization of the sampling oscilloscope is critical, otherwise the output signal calculated in MATLAB would be noisy. More details are described in Chapter 3 and Chapter 4.

Spectrum Measurement

Figure 2-17 shows the test setup for spectrum measurement with spectrum analyzer. SG1 and SG2 both output sinusoid signals. SG1 is the input signal and SG2 is the clock signal for the DUT.

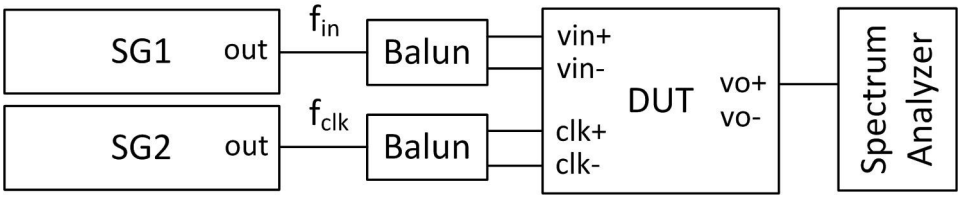


Figure 2-17: *Simplified test setup for spectrum measurement*

Spectrum measurement includes the measurement of SFDR, SNDR and THD. The ENOB of SNDR is a critical specification for the sampler and ADC. Equations (2-22)(2-23)(2-24) show how THD, SNDR and ENOB are calculated, where S indicates the signal power, N indicates the noise floor and D indicates the harmonic distortions.

$$THD = 20\log\frac{S}{D} \tag{2-22}$$

$$SNDR = 20\log\frac{S}{N+D} \tag{2-23}$$

$$ENOB = \frac{SNDR - 1.76}{6.02} \tag{2-24}$$

The spectrum analyzer calculates the FFT of the complete output signal including track and hold mode. However only the hold signal should be analyzed. The frequency span covers the first Nyquist zone. For the Nyquist sampling, the frequency of track signal is also inside the first Nyquist zone, therefore the spectrum result is not only for the hold signal. For the under-sampling, the track signal is in the higher Nyquist zone, only hold signal is in the first Nyquist zone, the spectrum result is precise for hold signal.

Another method of spectrum measurement uses the test setup in Figure 2-16 with sampling oscilloscope. The idea is to do resampling in MATLAB. The hold signal is resampled once in each sampling period [27]. This method ensures that only the hold signal is analyzed in the spectrum.

Resolution and full scale range of the ADC, i.e. the sampling oscilloscope, are n bit and V_{FS}, respectively. In order to test the THA we apply a sinosoidal signal with amplitude A and frequency f to its input. The analog input signal power is defined in Equation (2-29)

The signal digitized in the sampling oscilloscope suffers from the quantization noise and white noise of the oscilloscope as well as the clock jitter of the reference and trigger. All three factors raise the noise floor of the sampled signal in frequency domain. The following equations are taken from [9].

$$P_{err} = \frac{A^2}{2}(2\pi f \cdot \sigma_{jitter})^2 \tag{2-25}$$

$$P_q = (\frac{V_{FS}}{2^n})^2/12 \tag{2-26}$$

$$P_w = \sigma^2_{white} \tag{2-27}$$

$$NoiseFloor = P_{err} + P_q + P_w \tag{2-28}$$

$$P_{sig} = \frac{A^2}{8} \tag{2-29}$$

The power of the voltage error of a sine wave with amplitude A and frequency f due to the jitter of the sampling clock is given in Equation (2-25) with σ_{jitter} being the RMS jitter of the sampling clock of the oscilloscope. This jitter is caused not only by the oscilloscope itself but also the whole measurement setup. The power of the quantization noise for an ideal n bit ADC with the full scale range of V_{FS} is given by Equation (2-26). Furthermore, the sampling oscilloscope's broadband noise is given by Equation (2-27) assuming that the white noise has the RMS value of σ_{white}. It can be determined by building the whole setup without connecting the DUT and then measuring the output signal of the sampling oscilloscope. The theoretical noise floor of an ideal sine wave signal digitized in the oscilloscope is given by Equation (2-28). After the FFT analysis in MATLAB, the process gain has to be added to the FFT noise floor. The noise floor extends over the entire Nyquist bandwidth from DC to half of the sampling rate. The FFT works as a narrow-band spectrum analyzer with a bandwidth of f_s/M that sweeps over the spectrum, where f_s is the sampling rate and M is the size of FFT. It pushes the noise down which is the similar concept as the resolution bandwidth of spectrum analyzer. The process gain is defined in Equation (2-30). Equation (2-31) shows how to transfer $NoiseFloor_{FFT}$, the noise floor calculated by FFT, to the real noise floor value.

$$ProcessGain = 10 \cdot \log_{10}(\frac{M}{2}) \tag{2-30}$$

$$NoiseFloor_{dB} = NoiseFloor_{FFT} + ProcessGain \tag{2-31}$$

$$\tag{2-32}$$

In measurements with the spectrum analyzer, one principle to set the bandwidth resolution is that the noise floor should be low enough so that the harmonics are clear to observe. In this method, the noise floor is not only determined by the DUT itself, but also the test setup and process gain. Similarly, the process gain can be increased by increasing the length of the output signal to reveal the harmonics. However it is mentioned in Equation (2-23) that the noise floor is part of the consideration in SNDR calculation which yields the ENOB. Therefore it is important that the noise floor is influenced by the test setup as little as possible. The quantization noise of the sampling oscilloscope is low and fixed, but the jitter error caused by the synchronization can be larger when the input frequency becomes higher. One way to reduce this jitter error is to let sampling oscilloscope calculate average output. Although the jitter error would be covered but it is still changing with the frequency.

2.5 State of the Art in Ultra-broadband Sampling Circuits

Most of the broadband bipolar THAs are implemented in SEF topology which was first published by [29]. The bandwidth of an SEF THAs is limited by the emitter follower output resistance and the hold capacitor. Hence the bandwidth could be improved if a smaller hold capacitor could be used. However the lower limit of the hold capacitor value is set by the capacitor noise power kT/C [9] and the voltage droop in the hold mode. Thus the size of hold capacitor represents a trade-off between bandwidth, noise, and droop. Track-and-hold amplifiers (THA) in InP and SiGe heterobipolar (HBT) technology can achieve significantly higher bandwidth than CMOS THAs. In [30] a broadband THA in an InP HBT process is reported which achieved 70 GS/s sample rate and 51 GHz bandwidth. A 108 GS/s THA with 40 GHz of bandwidth was implemented in a 55nm SiGe BiCMOS technology and was reported in [31]. [32] reported a 25 GS/s SC based THA implemented in a 28 nm low-power CMOS process. A frequency compensation technique is employed to improve the bandwidth so that the small-signal bandwidth is 70 GHz and the large-signal bandwidth is 55 GHz.

Recently an electronic STI sampler with an IHC was demonstrated [27]. It presented a charge sampler for analog input in a 130 nm SiGe BiCMOS technology, with the sampling rate of 25.6 GS/s and 40 GHz large-signal 1dB-bandwidth. More than 5 ENOB and more than 33 dBc SFDR are achieved. A similar sampling technique was used in [21], however with an emphasis on using the integrator as an internal anti-aliasing filter and not as a broadband sampler.

The above mentioned publications are listed in Table 2-3 and represent the state of the art in ultrabroadband samplers.

A figure of merit (FoM) of a sampler or an ADC is usually calculated to reflect the design trade-off between the conversion speed, resolution and power consumption, the most classic definition is called Walden-FoM [33]. There are other variants of the FoM definitions [34], one modern FoM is Schreier-FoM [35], it includes the bandwidth as another design goal into the design trade-off. The equations of Walden-FoM and Schreier-FoM are shown in Equation (2-33)(2-34), where f_s is the sampling frequency, BW is the bandwidth and P is the power consumption.

$$FoM_w(J/conv.-step) = \frac{P}{2^{ENOB} \cdot f_s} \tag{2-33}$$

$$FoM_s(dB) = SNDR + 10\log\frac{BW}{P} \tag{2-34}$$

2.6 Conclusion

In this chapter, fundamental knowledge of sampling circuit including the overview of different sampling topologies, the comparison of multiple characteristics of different sampling system, and the measurement techniques for samplers are discussed.

The sampling technologies are categorized to TH and charge sampling. The popular topologies of TH sampling include switched-capacitor sampler, diode-bridge sampler,

Table 2-3: *State of the art.*

	[30]	[31]	[32]	[27]
Architecture	SEF	SEF	Switched capacitor	Charge sampling
Input amplitude	400 mVpp	160 mVpp	800 mVpp	500 mVpp
Max. sampling rate	70 GS/s	108 GS/s	25 GS/s	25.6 GS/s
Small-signal BW	51 GHz (3dB)	40 GHz (3dB)	70 GHz (3dB)	N/A
Large-signal BW	N/A	N/A	55 GHz (3dB)	40 GHz (1dB)
THD@f_{in}	-46dB@7GHz	-49dB@1GHz	-39dB@21GHz	-44dB@1GHz
ENOB@f_{in}	N/A	N/A	4.9@3GHz	6.4@1GHz
Power	N/A	87 mW	73 mW	913 mW
FoMw	N/A	N/A	98 fJ/conv.-step	422 fJ/conv.-step
FoMs	N/A	N/A	150 dB	147 dB
Die area	1.8 mm^2	0.49 mm^2	0.53 mm^2	1.5 mm^2
Process	130 nm InP DHBT	55 nm SiGe BiCMOS	28 nm CMOS	130 nm SiGe BiCMOS

and SEF sampler. The charge sampling technologies include photonic sampler and STI sampler. The core component of the charge sampling is the resettable integrator. The charge sampling for all electronic system using STI sampler is called as STI sampling.

The comparison of TH and STI sampler characteristics covers bandwidth, sampling jitter, noise, and droop. The bandwidth of TH sampler shows the characteristics of an RC filter, the bandwidth degrades with increasing the size of the hold capacitor. The characteristics of IHC bandwidth is an sinc function of integration time of the sampler, thus not related to the capacitor of the resettable integrator. Therefore the STI sampler has the advantage that its bandwidth is not limited by the capacitor. The jitter analysis of the STI sampling is done and compared to TH sampling, the result shows that they can provide similar performance due to the sampling jitter. The noise of the THA is highly depending on the hold capacitor, while IHC is not only affected by integration capacitance and temperature but also by integration and hold time. The droop of THA increases while reducing the size of the hold capacitor, therefore it is a trade-off between the bandwidth and droop. For the STI sampler, the droop of the integration capacitor is neglectable. This comparison shows that IHC has less limitation when selecting the capacitance because the integration capacitor is not related to the bandwidth or droop, and less related to the noise compared to the hold capacitor of THA. However, large integration capacitor will reduce the sampling rate of the STI sampling system using IHC. Based on this comparison we can see that STI sampler has advantage on several aspects compare to THA like bandwidth, noise, and droop.

Three measurement techniques for samplers are discussed based on S-parameter, transient, and spectrum measurements. The general test setups are presented. These techniques are able to offer thorough characterizing of a sampler from multiple aspects. S-parameters characterize mainly the small-signal bandwidth of the sampler. Transient and spectrum measurement run the sampler in the same way, while one is used to observe the sampler in time domain and the other shows the performance of the sampler in frequency domain.

The state of the art in ultra-broadband sampling circuits is introduced at the end. •

3 Design, Realization, and Measurement of an SEF-based Input-Buffer-Less THA

In this chapter, design, realization, and measurement of an SEF-based input-buffer-less THA are presented.

3.1 Preliminary considerations

In SEF THAs the input stage is usually realized with a differential amplifier as input buffer whereby the output resistor of the differential amplifier is used as pull-down resistor to control the base voltage of the switched emitter follower [36][31], as shown in Figure 3-1. However the differential amplifier with SEF load becomes a bandwidth bottleneck in the track mode, therefore a passive input stage is applied (see Figure 3-10).

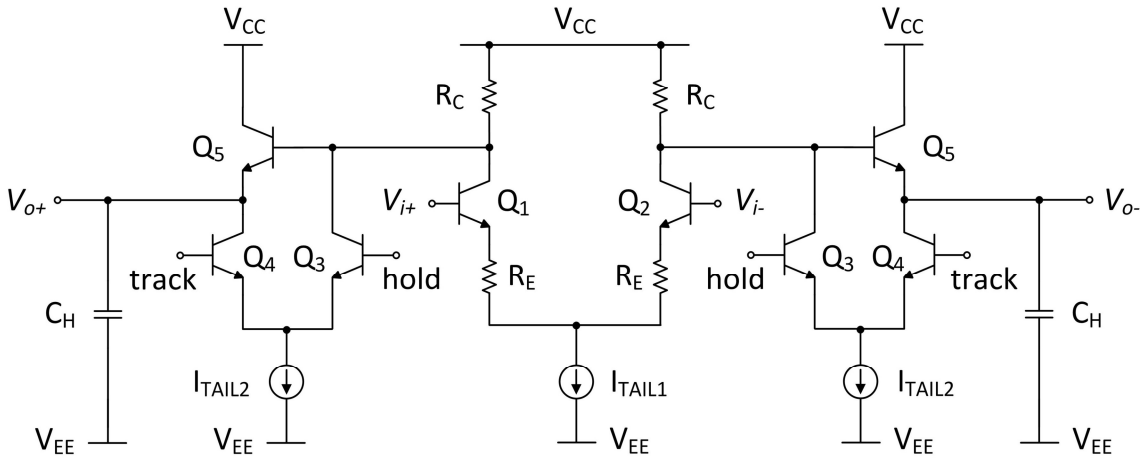
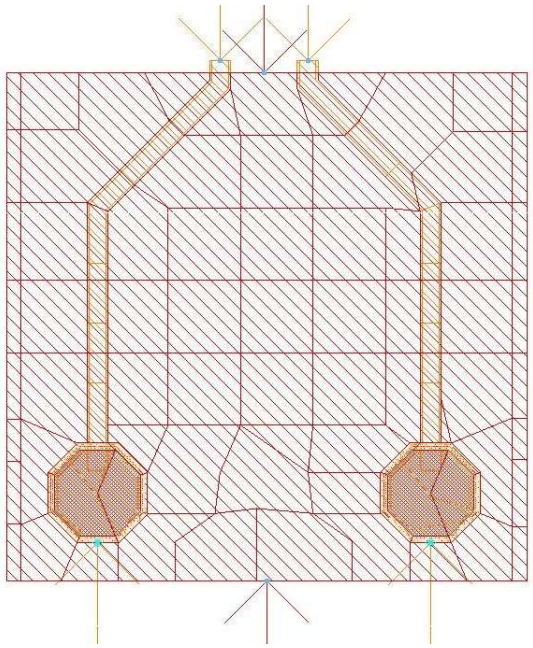


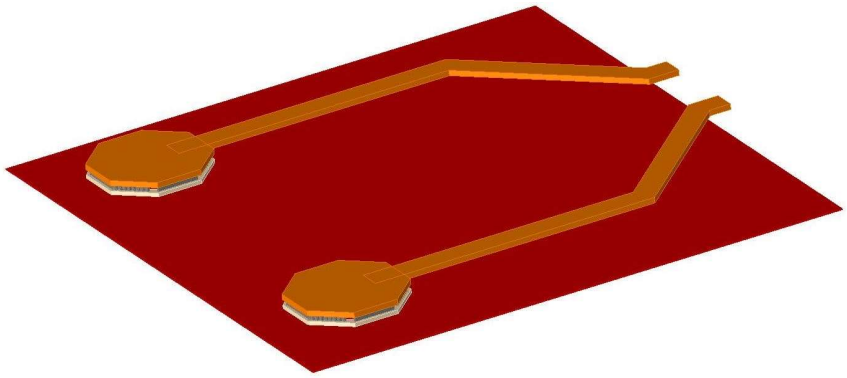
Figure 3-1: *Differential amplifier with SEF*

3.1.1 Microstrip Transmission Lines

The circuits in this work apply full-differential topology. Therefore, on-chip differential transmission lines (TLs) for differential inputs are designed. Since the distance between the differential input transistors are much shorter than the differential input pads, the coupling between the differential input signal lines are different. To ensure that the differential coupling is small, the differential input signal lines are designed in a way that the coupling is as small as possible. Therefore GSGSG pads are used to isolate the differential input pads from each other. At the transistor side, the distance between the differential transistors is six times of the transmission line. In such case, both odd and even mode 50 Ω impdedance matching can be achieved in common-mode and differential-operation. The TLs modeling and simulation are done using Momentum in ADS. Figure 3-2 shows the



(a)



(b)

Figure 3-2: *(a) Transmission line layout model (b) Transmission line 3D model*

transmission line layout and 3D model. The TL signal line uses layer top metal 2 while the ground is connected to the 3rd metal layer.

3.1.2 Inductive Peaking

Inductive peaking is often used to increase gain at higher frequencies to compensate the reduced gain above the 3dB bandwidth of the circuit. This broadband technique can be applied to either a passive or active input stage. Figure 3-3 shows how inductive peaking is applied to the 50 Ω input matching resistor. The signal generator (SG) is modeled with V_s and 50 Ω output matching resistor. V_B is the base voltage of Q_1, which is the first transistor receiving the input signal on the chip. TL is the microstrip transmission line, L_P is the peaking inductor. Equation (3-1) shows that the matching impedance works as a

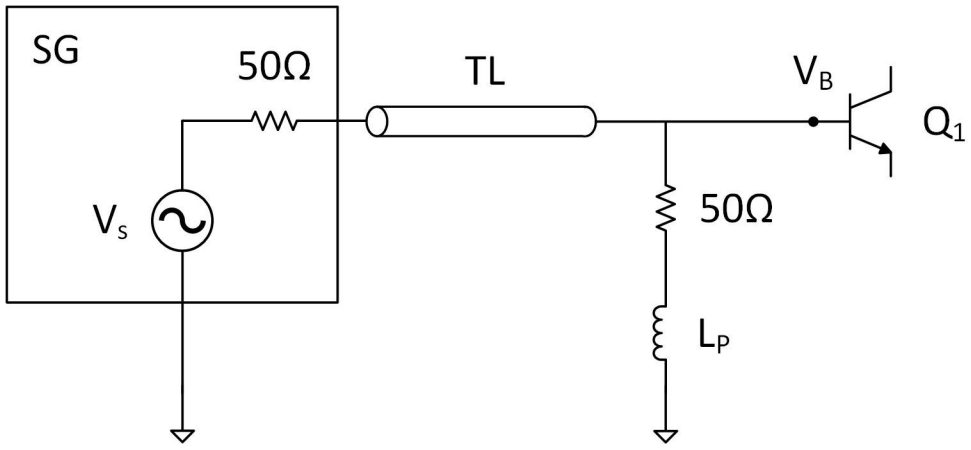


Figure 3-3: *Inductive peaking on the 50 Ω input matching resistor*

voltage divider. For low frequency, the inductor has low impedance, V_B is half of V_s. For high frequency, the inductor has high impedance, V_B is getting close to V_s. This inductor adds a zero to the whole circuit but the pole of the sampler is still dominant.

$$V_B = \frac{50\Omega + j\omega L_P}{100\Omega + j\omega L_P} V_s \tag{3-1}$$

The inductor was designed using Mühlhaus RFIC Inductor Toolkit in ADS [37]. The layout uses octagon differential center tap and can be seen in Figure. 3-12.

3.1.3 Emitter Follower

Figure 3-4 shows an emitter follower with capacitive load and its small-signal equivalent circuit. The transfer function is expressed in Equation (3-2). It shows similar behavior as an RLC resonant circuit [38]. The RLC circuit and the corresponding parameters like natural angular frequency, damping ratio and Q factor are shown in Figure 3-5 and Equation (3-3). If the Q factor is larger than $1/\sqrt{2}$, the circuit exhibits overshoot in time domain and peaking in frequency domain. Therefore over-design the 3dB bandwidth of the emitter follower above the specification is a common strategy in broadband circuit design. The overshoot is usually compensated by the layout parasitics.

$$\begin{aligned} \frac{1}{H(s)} &\approx s^2 \cdot \frac{r_b C_L}{\omega_T} + s \cdot \left(r_b C_\mu + \frac{r_b}{(R_E \parallel r_o)\,\omega_T} + C_L \left(\frac{r_b}{r_\pi g_m} + \frac{1}{g_m} \right) \right) + 1 \\ \omega_T &= \frac{g_m}{c_\pi + c_\mu} \end{aligned} \tag{3-2}$$

$$\begin{aligned} \omega_0 &= \frac{1}{\sqrt{LC}} = \sqrt{\frac{\omega_T}{r_b C_L}} \\ \delta &= \frac{R}{2L} = \left(\frac{c_\mu}{2C_L} + \frac{1}{2 r_b g_m} + \frac{1}{2\beta} \right) \omega_T + \frac{1}{2\,(R_E \parallel r_o)\,C_L} \\ Q &= \frac{\omega_0}{2\delta} \end{aligned} \tag{3-3}$$

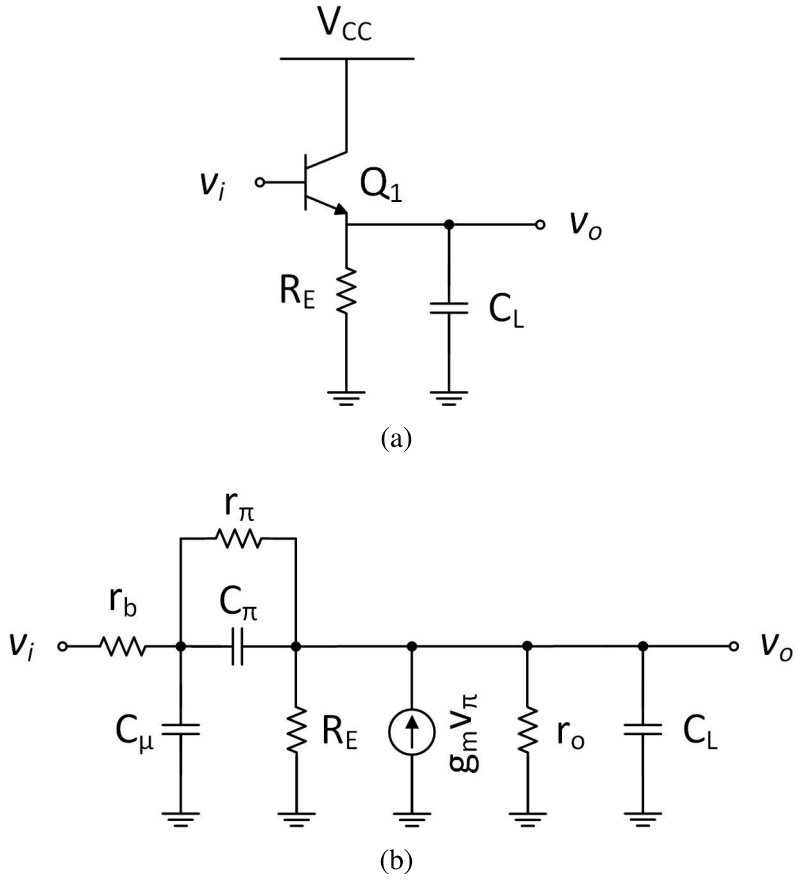


Figure 3-4: *(a) Emitter follower with capacitive load (b) Small-signal equivalent circuit of emitter follower with capacitive load*

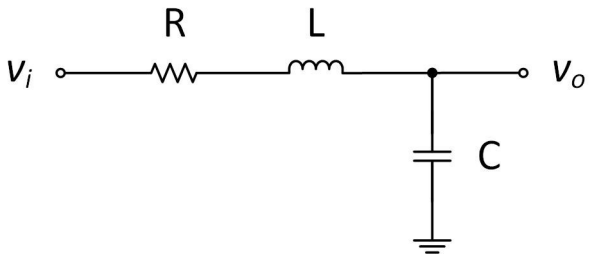


Figure 3-5: *RLC resonant circuit*

3.1.4 Differential Amplifier

The design of the output buffer needs to meet several requirements such as high gain, high linearity, and large bandwidth. In this design, the differential amplifier is selected as the topology for the output buffer. Figure 3-6 shows the differential amplifier with emitter degeneration and cascode structure [39].

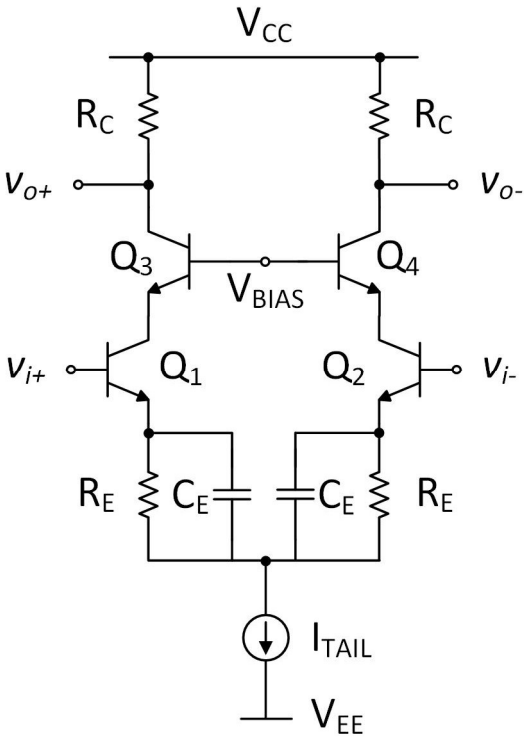


Figure 3-6: *Differential amplifier with emitter degeneration and cascode stage*

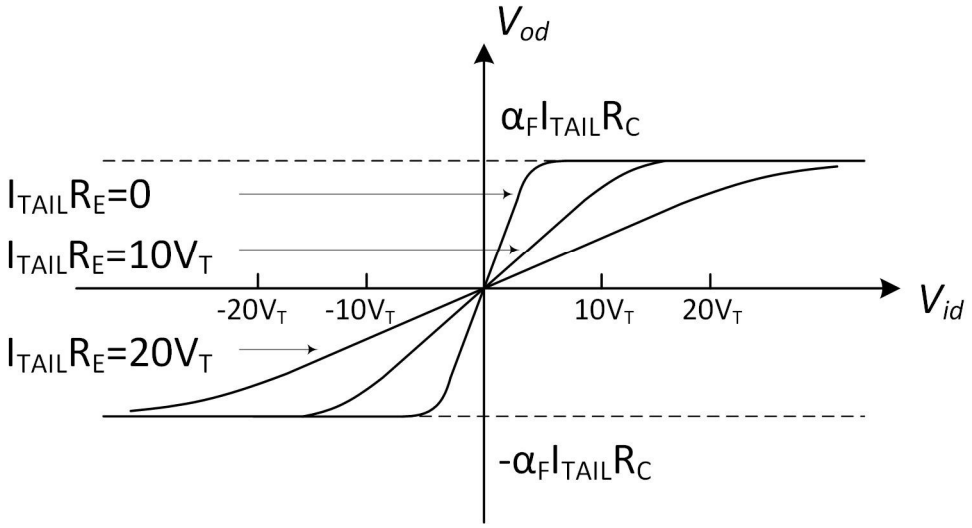


Figure 3-7: *Differential DC transfer characteristic of the differential amplifier with emitter degeneration and $I_{TAIL}R_E$ as parameter*

Emitter Degeneration

The differential output without emitter degeneration is expressed in Equation (3-4).

$$V_{od} = \alpha_F I_{TAIL} R_c \tanh\left(\frac{-V_{id}}{2V_T}\right) \tag{3-4}$$

When increasing the range of V_{id}, the linearity of the amplifier starts to reduce. With the emitter-degeneration resistor R_E, the linear range of the operation is extended approximately to $I_{TAIL}R_E$ [39]. When one transistor is off, I_{TAIL} flows in one degeneration resistor, this means the value of V_{id} required to turn one transistor off is changed by the voltage drop on R_E. The DC transfer characteristic is shown in Figure 3-7.

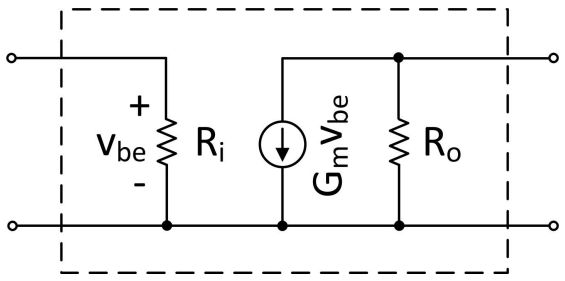


Figure 3-8: *Two-port small-signal equivalent of emitter-degenerated common-emitter amplifier [39]*

Figure 3-8 shows the two-port small-signal equivalent of emitter-degenerated common-emitter amplifier, with the approximation of $\beta_0 \gg 1, r_o \gg R_E, g_m r_o \gg 1$. Emitter degeneration reduces the transconductance, increases the input and output resistance as shown in Equation (3-5) [39].

$$\begin{aligned} G_m &\simeq \frac{g_m}{1 + g_m R_E} \\ R_i &\simeq r_\pi + (\beta_0 + 1) R_E \\ R_o &\simeq r_o (1 + g_m R_E) \end{aligned} \tag{3-5}$$

Common-Base Amplifier

Transistors $Q_{3,4}$ construct the differential common-base stage of the amplifier. As long as the output resistance of the cascode transistor is large compared to the load resistance R_C, the common-base stage does not affect the voltage gain of the amplifier. The cascode amplifier has advantage at high frequencies. Since Q_1 and Q_3 have the same bias current and device dimensions, their transconductance are equal. The load of Q_1 is the input impedance of the common-base amplifier, approximately $1/g_{m3}$, therefore the voltage gain of Q_1 is about unity, which minimize the influence of the Miller effect on Q_1. Since the common-base stage itself has also a wide bandwidth, the overall circuit has good high-frequency performance [39].

Bandwidth Analysis

The AC differential half-circuit of the cascode amplifier and its small-signal equivalent circuit are depicted in Figure 3-9. Due to the complexity of the circuit, it is hard to calculate the formula for the gain to find the bandwidth. An approximate method, the so called zero-value time constant analysis, can be used [39]. It helps to find the dominant pole which yields the bandwidth of the circuit. The zero-value time constant is based on the analysis of the resistance seen from each capacitor. This circuit has in total 6

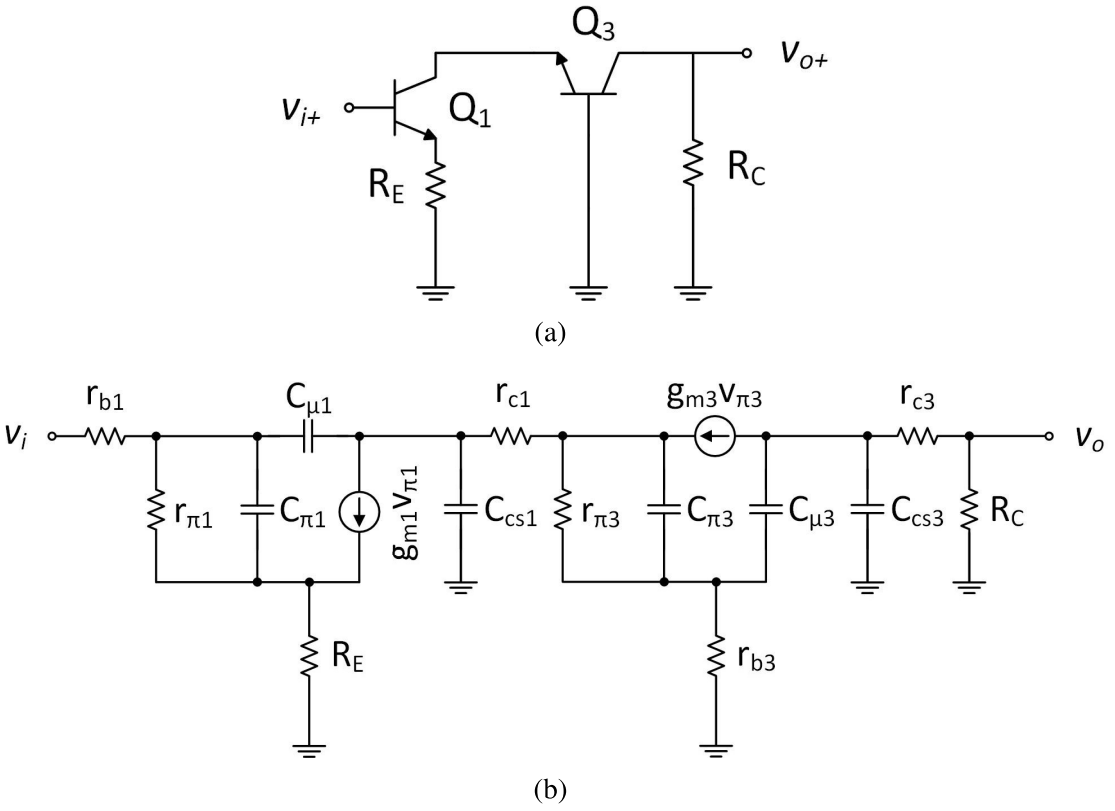


Figure 3-9: *(a) AC differential half-circuit (b) Small-signal equivalent circuit*

capacitors. The 3dB bandwidth is expressed in Equation (3-6). Emitter degeneration R_E reduces $R_{\pi 1}$, thus increases the bandwidth by reducing the zero-value time constant with $C_{\pi 1}$. Therefore R_E increases the bandwidth contribution of Q_1 and Q_3 adds extra bandwidth contribution as shown in Equation (3-6).

$$
\begin{aligned}
R_{\pi 1} &= r_{\pi 1} \parallel \frac{r_{b1} + R_E}{1 + g_{m1} R_E} \\
R_{cs1} &= R_{i3} + r_{c1} = \frac{1}{g_{m3}} + \frac{r_{b3}}{\beta + 1} + r_{c1} \\
R_{\mu 1} &= (r_{\pi 1} + (\beta + 1) R_E) \parallel r_{b1} + R_{cs1} + G_{m1}((r_{\pi 1} + (\beta + 1) R_e) \parallel r_{b1}) R_{cs1} \\
R_{\pi 3} &= r_{\pi 3} \parallel \frac{1}{g_{m3}} \\
R_{\mu 3} &= r_b + r_{c3} + R_C \\
R_{cs3} &= r_{c3} + R_C \\
\Sigma T_0 &= R_{\pi 1} C_{\pi 1} + R_{cs1} C_{cs1} + R_{\mu 1} C_{\mu 1} + R_{\pi 3} C_{\pi 3} + R_{\mu 3} C_{\mu 3} + R_{cs3} C_{cs3} \\
f_{3dB} &= \frac{1}{2\pi \Sigma T_0}
\end{aligned}
\tag{3-6}
$$

Peaking Techniques

Capacitive and inductive peaking are two peaking techniques often used in differential amplifiers. The idea of capacitive peaking is to put peaking capacitor C_E parallel to R_E,

so that R_E is replaced to $R_E \parallel \frac{1}{sC_E}$. When the frequency increases, C_e reduces the emitter impedance, which will increase the gain of the amplifier thus compensate the gain loss at high frequency. Inductive peaking has similar concept, it puts peaking inductor L_C series to R_C, replaces R_C to $R_C + sL_c$. As the frequency increases, L_C increases the collector impedance, thus increases the gain of the amplifier at high frequency. Both of them show zero on the frequency response of the amplifier.

3.2 Schematic Analysis and Design

The complete schematic of the THA is shown in Figure 3-10. The THA operates fully differential with differential signal input (vi+, vi-), differential clock input (track, hold), and differential signal output (vo+, vo-). The high-frequency inputs and outputs are connected to on-chip microstrip transmission lines and are terminated with 50 Ω resistors near the transistors. The microstrip transmission lines are built from thick top metal for the signal and low metal layer (3rd metal) for ground.

3.2.1 SEF as Input Stage

In this circuit, the differential input amplifier in the traditional SEF design is removed, and the SEF itself is used as input buffer with the 50 Ω resistor being the pull-down resistor for the emitter follower. The SEF core is constructed with one emitter follower Q_7 and two current switches $Q_{8,9}$ and $Q_{11,12}$ with the size of 140/900 nm. The tail current for Q_7 and $Q_{8,9}$ is set to 4 mA. This current switch turns the emitter current of Q_7 off during the hold mode. The other current switch $Q_{11,12}$ with the size of 140/900 nm switches a large tail current of 30 mA. This current flows through the 50 Ω resistor to create sufficiently large pull down voltage for the SEF to pull down the base voltage of Q_7. Using such a large pull down current is required to isolate the input signal during the hold mode in order to minimize feedthrough and droop. To further reduce the feedthrough during the hold mode, capacitor C_{FT} constructed by four transistors with the size of 140/900 nm is cross-coupled to the input and output of the differential SEFs [36]. Since the sizes of both the 50 Ω resistor and Q_{11} become large to allow enough pull-down current and avoiding electromigration, the parasitic capacitance at the input node is increased. Therefore inductor L_P is added at the input to allow for inductive peaking at high frequencies. The size of $Q_{11,12}$ is 700/900 nm. We used two separate current switches ($Q_{8,9}$, $Q_{11,12}$) in order to have separate control for the switching of the base voltage and emitter current of Q_7. Hence Q_7 and C_{FT} can be set to small sizes. This reduces parasitic capacitance of the switch and improves bandwidth while decreasing leakage current in the hold capacitor.

The size of the hold capacitor C_H is chosen to be 30 fF. For small-signal noise analysis the SEF with hold capacitor behaves similar as a first order RC filter and its noise can be modeled as kT/C [9]. The size of the hold capacitor has to be set as a compromise between bandwidth and noise. The broadband noise analysis in the post layout simulation yields an RMS noise of 0.5 mV, 75% of it is from kT/C. This is lower than the broadband noise of the sampling oscilloscope used during the measurement.

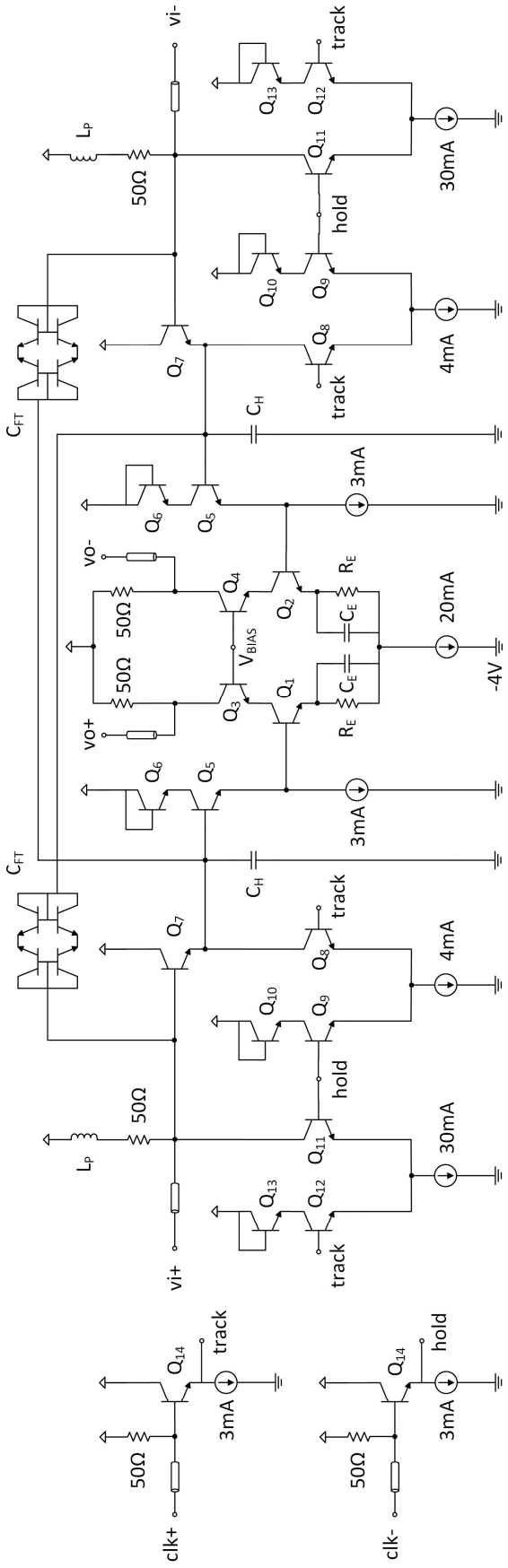


Figure 3-10: *Schematic of SEF-based buffer-less THA*

3.2.2 Output Buffer

The output buffer is a differential amplifier $Q_{1,2}$ with cascode transistors $Q_{3,4}$, their size are 700/900 nm. Since the collector resistor is set to 50 Ω, both emitter degeneration resistance R_E and large tail current of 20 mA are applied to achieve a good linearity. R_E is set to 18 Ω. Total Harmonic Distortion (THD) is a major concern when calculating the ENOB from Spurious-Free Dynamic Range (SFDR). The emitter degeneration and large tail current guarantees at least -49 dB THD for 450 mVpp in the post layout simulation. Peaking capacitance C_E is applied to test the track mode bandwidth, otherwise the bandwidth during the track mode would be limited by the output buffer and could not be measured. However, capacitive peaking in the output stage is only used to tune out the bandwidth limitation of the output buffer, not to extend the overall bandwidth. Another emitter follower Q_5 with the size of 140/900 nm is used as middle stage before the output buffer. The size and bias of Q_5 is smaller than $Q_{1,2}$, so that the leakage current in the hold capacitor is reduced.

3.2.3 Power Dissipation

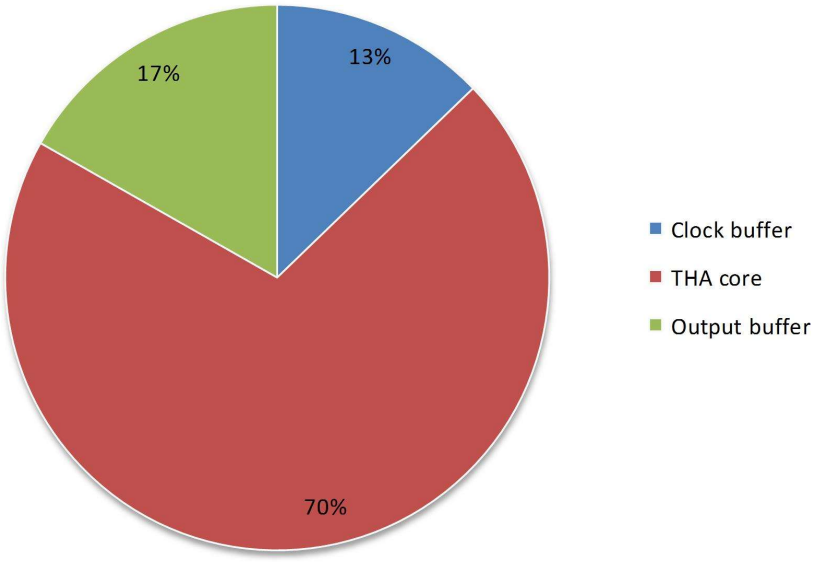


Figure 3-11: *Power consumption breakdown chart.*

The power supply was chosen to -4 V. The current consumption is 110 mA. Thus the DC power is 440 mW. The power dissipation breakdown chart is shown in Figure 3-11. The high power consumption is mainly due to three reasons. The first reason is that the pull-down current is very large to put the circuit in the hold mode. The second reason is that there are CML switches used to control the circuit operation mode while generally bipolar CML is power hungry. The third reason is that differential amplifier is used as output buffer, and higher current through the differential amplifier is needed to achieve higher linearity and bandwidth. In addition, more voltage is needed between VCC and VEE to design differential cascoded amplifier with emitter degeneration, which also brings more linearity and bandwidth. Therefore the supply voltage of -4 V was applied.

3.3 Layout and Chip

Figure 3-12 shows the layout of the THA core with buffers. The main components of the design are marked in the figure. Special care was taken to design all differential high-speed circuitry perfectly symmetric and as compact as possible. The active area including the inductance is only 230 x 200 um^2. The peaking inductance for the input signal is implemented by means of an octagonal differential inductor with a center tap connected to the supply as explained earlier.

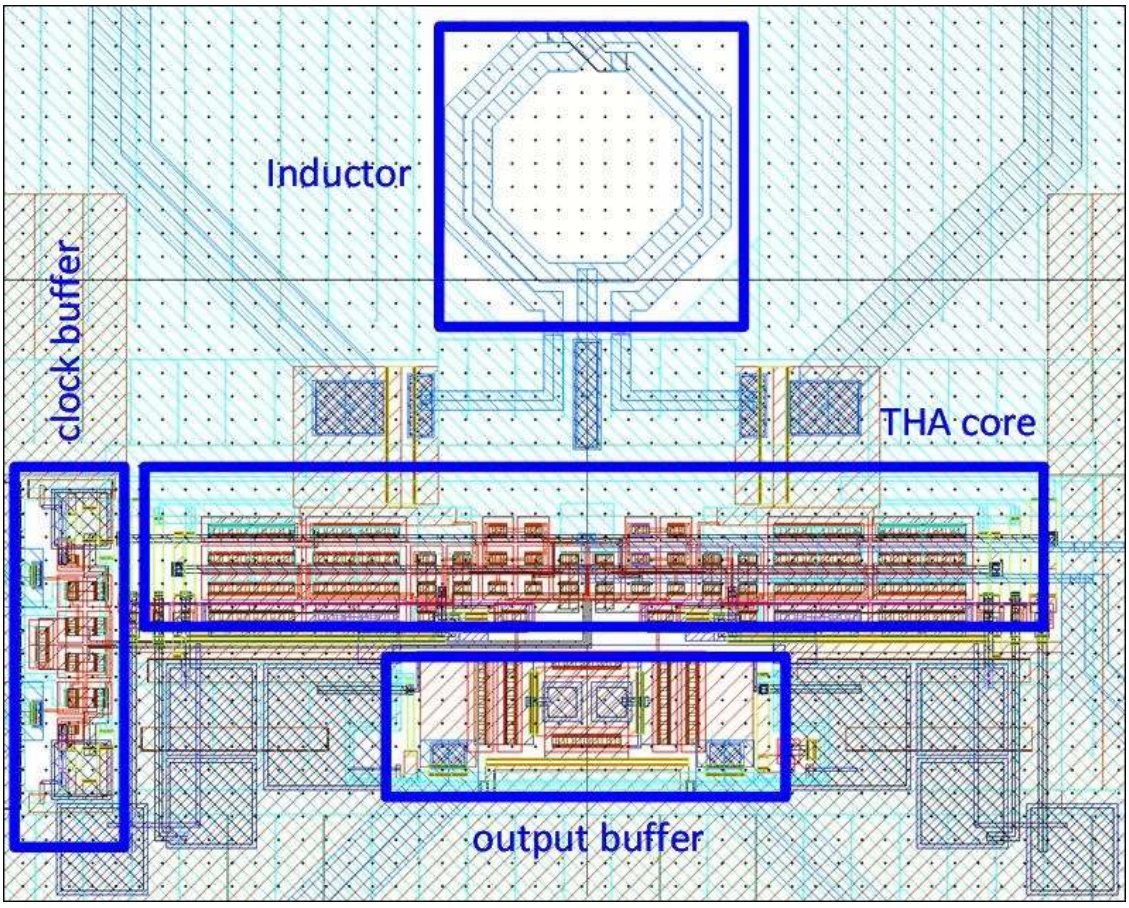


Figure 3-12: *Layout of THA core*

The chip is fabricated in a 130 nm SiGe BiCMOS technology from IHP (SG13G2) featuring high-speed Silicon Germanium heterobipolar transistors with cut-off frequencies of f_T/f_{max} = 300/500 GHz [40]. Figure 3-13 shows the micro-photograph of the chip. The chip size is 0.79 mm^2. The GSGSG pads at the upper and lower side are used for probing input and output signal, respectively. The clock signal for track and hold at left side is probed with GSSG pads. The on-chip microstrip transmission lines are separated by a distance of at least 3 times of the signal line width to have minimum coupling between them. The DC pads are located at the chip corners.

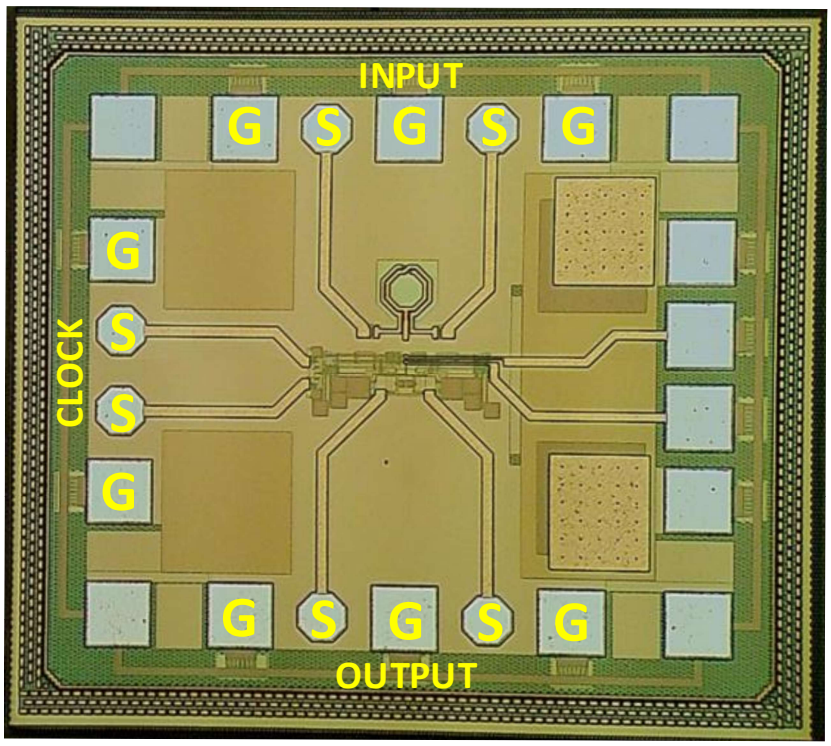


Figure 3-13: *THA chip micro-photograph*

3.4 Measurement Results

The measurement is done in both frequency domain (S-parameters) and time domain. The input and output GSGSG pads on the chip are contacted with Infinity probes. In frequency domain, the chip was measured with a static sampling clock signal separately for hold mode and track mode to obtain track mode bandwidth and hold mode feed-through. In time domain, the chip was measured with a high-speed clock signal using a sampling oscilloscope and a spectrum analyzer.

3.4.1 RF Module

The RF module is shown in Figure 3-14. The PCB is made from an Isola Tera substrate which was mounted onto a copper plate. The chip was placed into a cavity in the substrate to keep the bond wires between chip and substrate as short as possible. The positive and negative clock signal were wire-bonded to a microstrip transmission line or probed using direct on-chip probing, depending on the experiment. All RF inputs, outputs, and clock signals are terminated on-chip with 50 Ω. The RF differential input and output signals were not bonded. Instead, on-chip probing was applied.

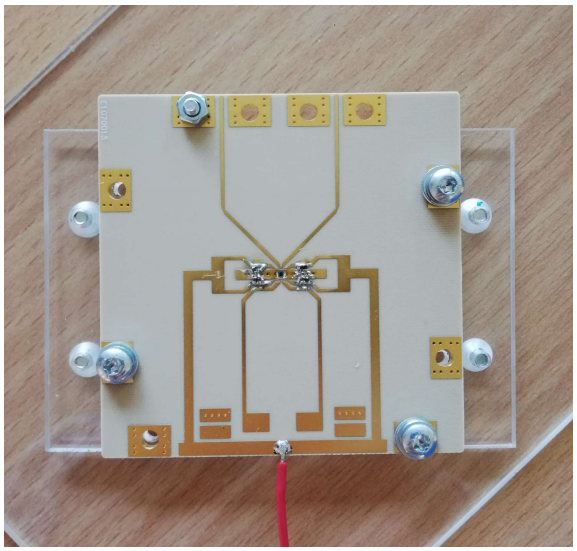


Figure 3-14: *RF module.*

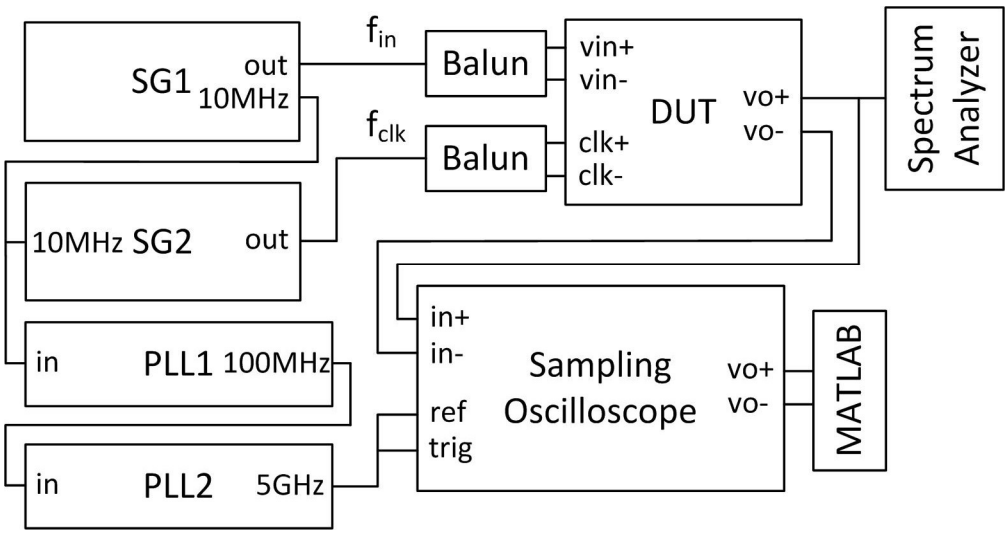


Figure 3-15: *Test setup for transient and spectrum measurement*

3.4.2 Test Setup

Figure 3-15 is the test setup for transient and spectrum measurement. SG1, Anritsu MG3694, is used to generate the input signal. SG2, Rohde & Schwarz 1035-5005-04, generates the clock. The sampling oscilloscope used here is Keysight 86100D DCA-X with wide bandwidth of 70 GHz. It digitizes the output of the DUT. The spectrum analyzer is an Anritsu MS2760A. It analyzes the spectrum of the hold signal. SG1 and SG2 are synchronized with internal 10 MHz reference clock of SG2. In order to synchronize all the test equipment together, the same reference clock is also applied as the reference input for PLL1 and PLL2, the output of the PLL1 and PLL2 is used as the reference and trigger of the sampling oscilloscope. PLL1 is Linear DC1795A [41], a low-phase-noise PLL using a low-frequency VCSO (voltage-controlled SAW oscillator). PLL2 is TI LMX2594EVM [42], a low-phase-noise PLL provides programmable high-frequency clock. PLL1 filters the noisy 10 MHz synchronization signal from the SG1. The advan-

tage of PLL1 is that it has an 1 GHz VCXO and narrow loop filter bandwidth. PLL1 outputs 100 MHz signal to PLL2. PLL2 outputs either 5 GHz to the reference and trigger of the sampling oscilloscope, which can enable precision timebase (PTB) function to make sure that the measured signal has minimum phase noise with good synchronization between DUT and sampling oscilloscope. The differential output of the sampling oscilloscope is calculated manually in MATLAB. The broadband noise power of the oscilloscope can be measured by attaching 50 Ω to the ports of the oscilloscope and measuring the transient signal. The transient noise signal is imported into MATLAB and calculated to be RMS 1.5 mV.

3.4.3 Test Environment

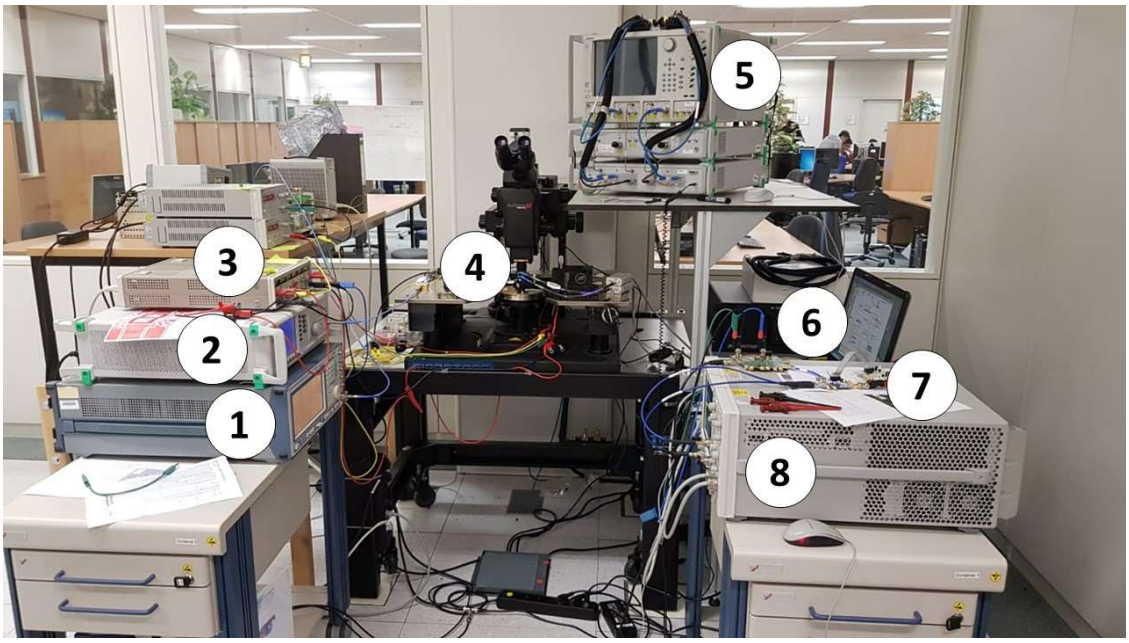


Figure 3-16: *Test environment in the lab*

Figure 3-16 shows the test environment in the lab. The test equipments are marked in the figure and explained as follows.

1. Signal generator, Rohde & Schwarz 1035-5005-04, it is used as clock input during the measurement when higher sampling rates are measured.
2. Signal generator, Anritsu MG3694, it is used as input signal. The 10 MHz internal oscillator is used as synchronization source for all the other devices.
3. DC voltage source, they are used as power supply and bias DC voltage for the chip.
4. Probe table equipped with Infinity probe from CASCADE with GSGSG 100 um pitch up to 110 GHz.
5. VNA, Anritsu VNA MS4647b for the S-parameter measurement.
6. Spectrum analyzer, Anritsu MS2760A, a portable device connected with laptop.

7. PLLs, Linear DC1795A and TI LMX2594EVM. They are used for low frequency sampling clock input and synchronization signal for the sampling oscilloscope.

8. Sampling oscilloscope, Keysight 86100D DCA-X, it measures and saves the transient output signal, then the data is analyzed and plotted in MATLAB.

Another signal generator Keysight E8257D is not shown in the figure, it represents a signal source with frequency range up to 70 GHz, therefore it is used when high frequency input signal are tested.

3.4.4 S-Parameter Measurement

The chip was first tested with a broadband vector network analyzer (VNA, Anritsu VNA MS4647b) to measure the small signal performance in track and hold mode separately. The test setup is shown in Figure 2-15. Figure 3-17 shows the single-ended measurement results from 1 to 70 GHz. For both input and output, one of the differential ports was terminated with 50 Ω resistor, therefore single-ended measurements were performed. The chip is set either in track mode or hold mode using a static clock signal. The gain of the S_{21} in track mode is -6 dB, thus the chip gives unity gain in the differential mode as intended. The 3dB cut off frequency is around 70 GHz indicating very high bandwidth. The small peak in the frequency response can be attributed to inductive peaking at the THA input. The S_{21} in hold mode gives at least -30 dB attenuation indicating very good hold mode feedthrough suppression. The S_{11} and S_{22} for the input and output ports during the track mode are also plotted. Both of them show less than -10 dB reflection up to 40 GHz.

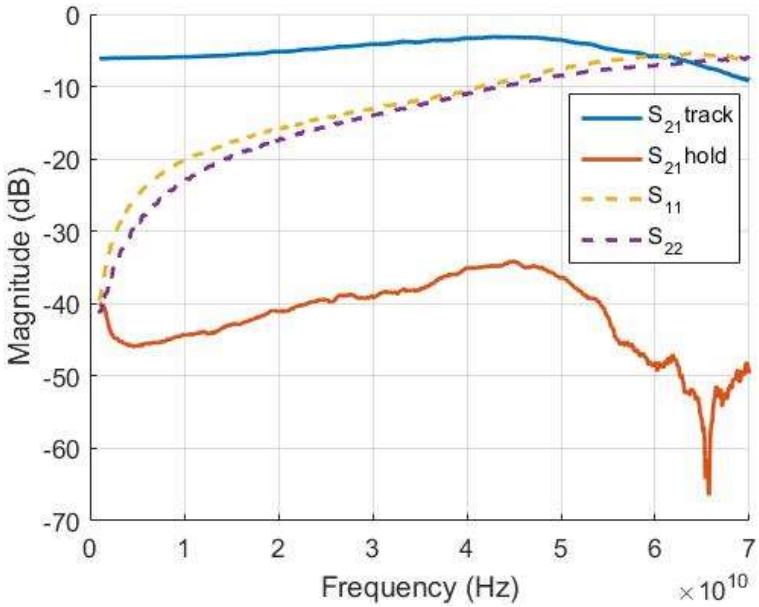
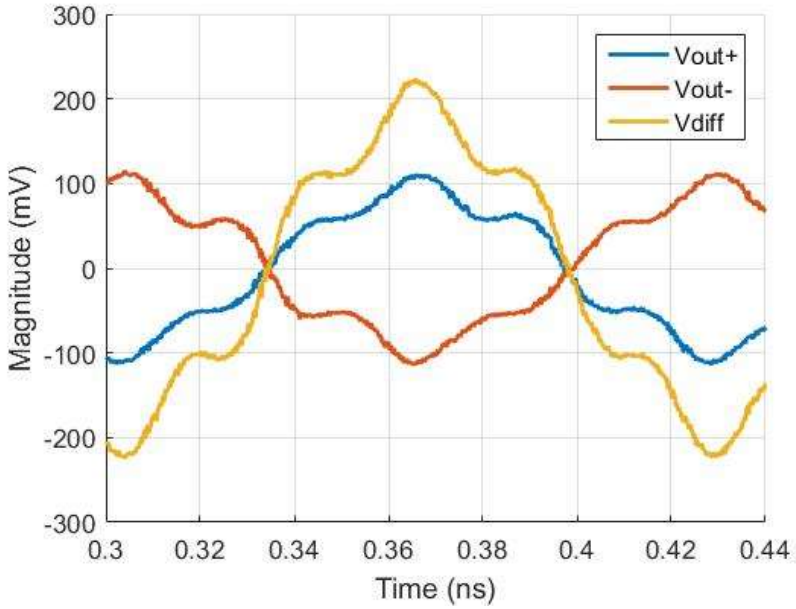
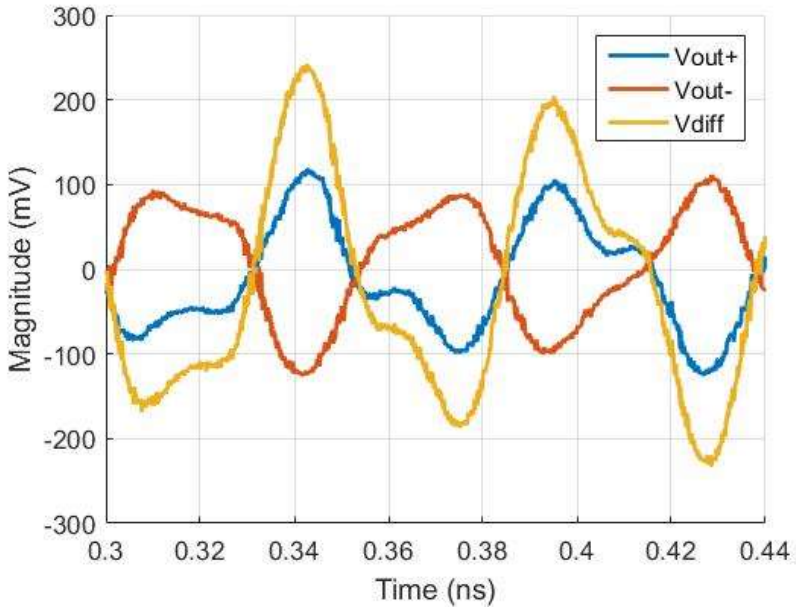


Figure 3-17: *S-parameter measurement results of the THA chip [A1]*

3.4.5 Transient and Spectrum Measurement



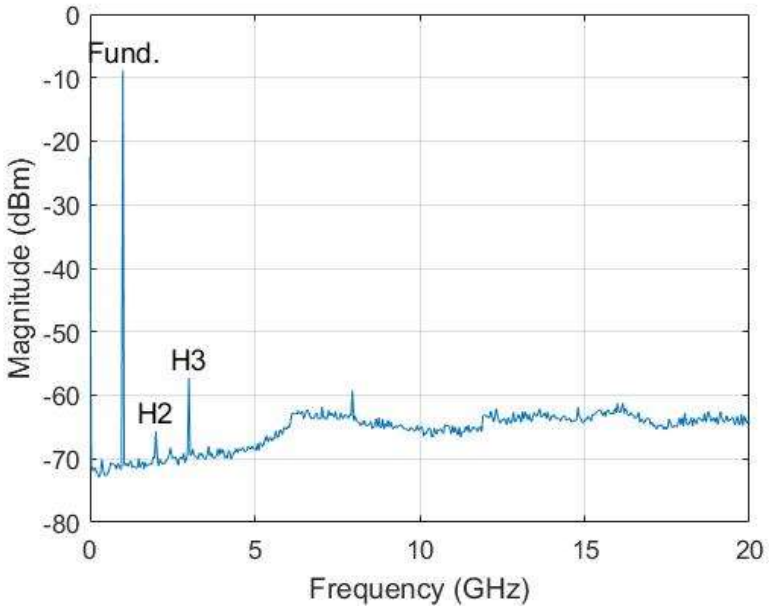
(a)



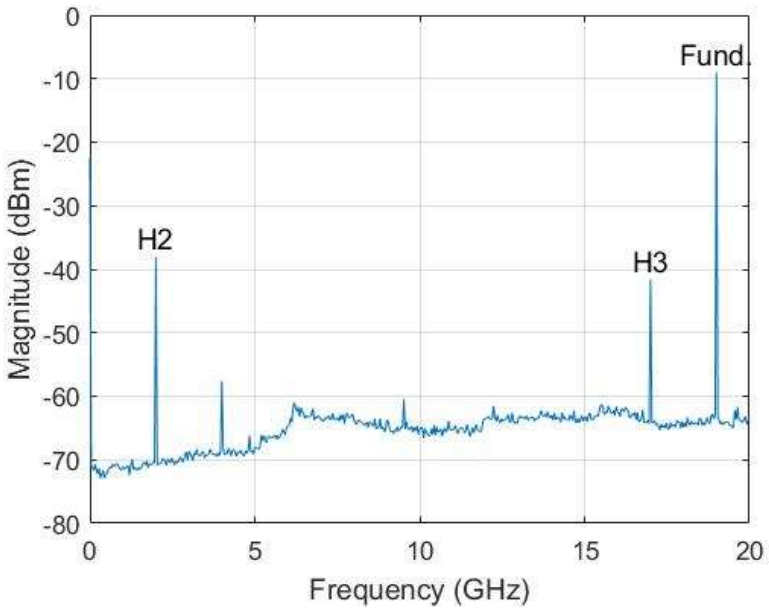
(b)

Figure 3-18: *Measured output signal of 450 mVpp (a) 8 GHz (b) 18 GHz differential input sampled by 40 GS/s clock [A1]*

The transient signal is measured with both spectrum analyzer and oscilloscope. The test setups are shown in Figure 2-16 and Figure 2-17. The main test equipment in this setup is the signal generator 1 (SG1, Anritsu MG3694), signal generator 2 (SG2, Rohde & Schwarz 1035-5005-04), the PLLs (Linear DC1795A, TI LMX2594EVM), the spectrum analyzer (Anritsu MS2760A), and the sampling oscilloscope (Keysight 86100D DCA-X).



(a)



(b)

Figure 3-19: *Spectrum of single ended output signal of (a) 1 GHz (b) 19 GHz differential input sampled by 40 GS/s clock [A1]*

All signal generators and the PLLs are synchronized to each other. SG1 is used to generate the input signal for the device under test (DUT, THA), SG2 generates the sampling clock for the DUT, the sampling oscilloscope digitizes the output of the DUT. The output of the PLLs provides low phase noise programmable high-frequency trigger clock to the sampling oscilloscope.

The sampling rate is 40 GS/s, with 40 GHz being the maximum frequency of SG2. The input frequency extends from 1 to 20 GHz as the Nyquist zone of the applied sampling

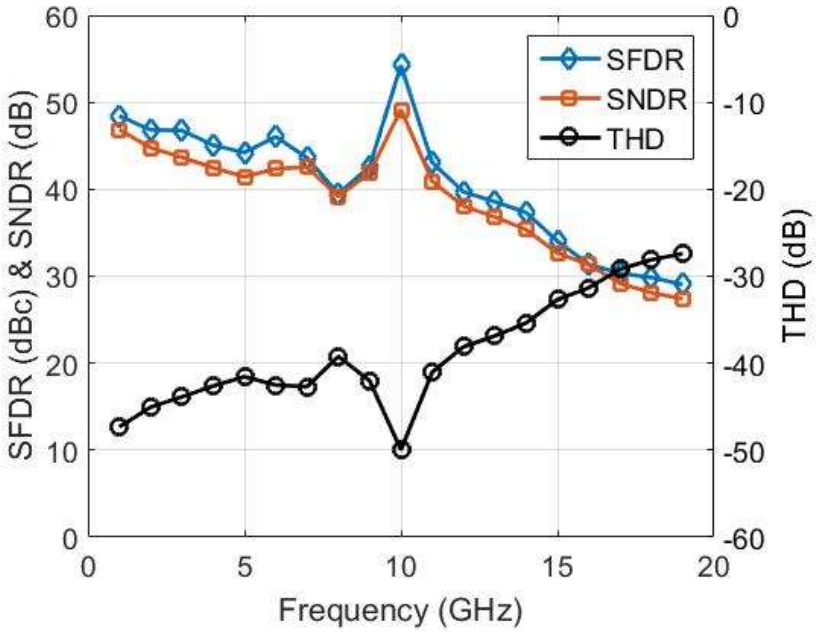


Figure 3-20: *SFDR, SNDR, THD vs. input frequency by 40 GS/s clock [A1]*

rate.

Figure 3-18 shows the differential 450 mVpp amplitude input signal with the frequency of 8 GHz and 18 GHz sampled by 40 GS/s clock. The figure shows the raw data of the positive and negative output signal from the oscilloscope. The differential output is calculated with MATLAB.

The white noise of the chip is measured by providing only DC supply to the DUT and measuring the transient signal. The transient noise signal is imported into MATLAB and calculated to be RMS 1.6 mV. Applying the deconvolution of the measured chip noise and the test setup noise, the broadband noise of the chip is RMS 0.6 mV. With the signal power of 450 mVpp, the ENOB of SNR is 7.8 bit.

The single ended output of 1 GHz and 19 GHz input sampled at 40 GS/s is measured with the spectrum analyzer shown in Figure 3-19. The test setup is shown in Figure 2-17. The frequency span is the corresponding Nyquist zone of 20 GHz, the resolution bandwidth of the spectrum analyzer is 10 kHz. For 1 GHz input, the output signal shows the best harmonic distortion performance that HD3 is -48 dB as the worst spur. For 19 GHz input, the HD2 and HD3 are the dominant harmonics, which locate at 2 GHz and 17 GHz respectively.

Figure 3-20 represents the SFDR, SNDR and THD vs. frequency at 40 GS/s clock. The SFDR reduces with the increasing frequency. The best case THD is at 1 GHz with -47 dB, while SFDR is 48 dBc and SNDR-related ENOB is 7.5 bit thus the THA resolution is limited by THD rather than broadband noise. The SFDR drops to 34 dBc at 15 GHz, while the ENOB is 5 bit. 10 GHz input is not counted for the performance because its harmonics are not captured.

3.5 Conclusion

This chapter presents an SEF-based input-buffer-less differential THA using 130 nm SiGe BiCMOS technology [A1]. The fundamental techniques of designing a broadband SEF THA circuit including transmission line, peaking techniques, emitter follower, and differential amplifier are discussed. The detailed measurement setup for large-signal measurement is introduced. The small-signal 3dB bandwidth of the THA is around 70 GHz. Sampling the input signal at 40 GS/s yields a peak SNDR-related ENOB of 7.5 bit at 1 GHz, and of >5 bit up to 15 GHz. A comparison of this chip to the state of the art of sampling circuits is shown in Table 3-1. Our THA shows the largest bandwidth of any THA published so far. The sampling rate limitation is due to limitations of our measurement equipment. With the input-buffer-less SEF THA topology excellent performance with respect to sampling rate, bandwidth, hold-mode feedthrough, and linearity is achieved.

Table 3-1: *Comparison to the state of the art.*

	[31]	[32]	[27]	[A1]
Architecture	SEF	Switched capacitor	Charge sampling	SEF
Input amplitude	160 mVpp	800 mVpp	500 mVpp	450 mVpp
Max. sampling rate	108 GS/s	25 GS/s	25.6 GS/s	40 GS/s
Small-signal BW	40 GHz (3dB)	70 GHz (3dB)	N/A	70 GHz (3dB)
Large-signal BW	N/A	55 GHz (3dB)	40 GHz (1dB)	19 GHz (3dB)
THD@f_{in}	-49dB@1GHz	-39dB@21GHz	-44dB@1GHz	-47dB@1GHz
ENOB@f_{in}	N/A	4.9@3GHz	6.4@1GHz	7.5@1GHz
Power	87 mW	73 mW	913 mW	440 mW
FoMw	N/A	98 fJ/conv.-step	422 fJ/conv.-step	61 fJ/conv.-step
FoMs	N/A	150 dB	147 dB	153 dB
Die area	0.49 mm^2	0.53 mm^2	1.5 mm^2	0.79 mm^2
Process	55 nm SiGe BiCMOS	28 nm CMOS	130 nm SiGe BiCMOS	130 nm SiGe BiCMOS

4 Design, Realization, and Measurement of an SEF-based THA with Input Buffer

In this chapter, an improved version of the SEF THA from Chapter 3 is presented.

4.1 Preliminary considerations

The input-buffer-less SEF THA presented in the previous chapter shows excellent small-signal bandwidth, however the large-signal bandwidth is still limited. The reason is that the SEF itself is not broadband enough to offer fast sampling. In this chapter, a differential amplifier is used as buffer for the SEF, the bandwidth of the SEF with holding capacitor is also extended.

4.1.1 Bandwidth Extension on the Emitter Follower

Figure 4-1 shows the emitter follower with collector inductor and its small-signal equivalent circuit. [43] introduces fast analytic circuits techniques (FACTs) to analyze the transfer function of the circuit, without giving too much effort and ignore the non-critical factors. The idea is to find the low-entropy form of the transfer function. Equation 4-1 shows a typical low-entropy form of the transfer function, only the DC gain H_0, dominant zero ω_z and pole ω_p are needed.

$$H(s) = H_0 \frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{\omega_p}} \tag{4-1}$$

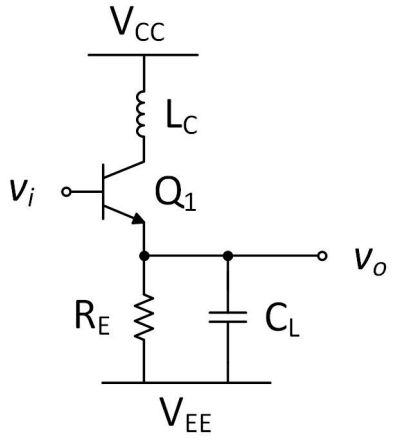
The DC gain is obtained by shorting inductor and opening capacitors of the small-signal equivalent circuit.

$$H_0 = \frac{g_m R_E}{1 + g_m R_E} \tag{4-2}$$

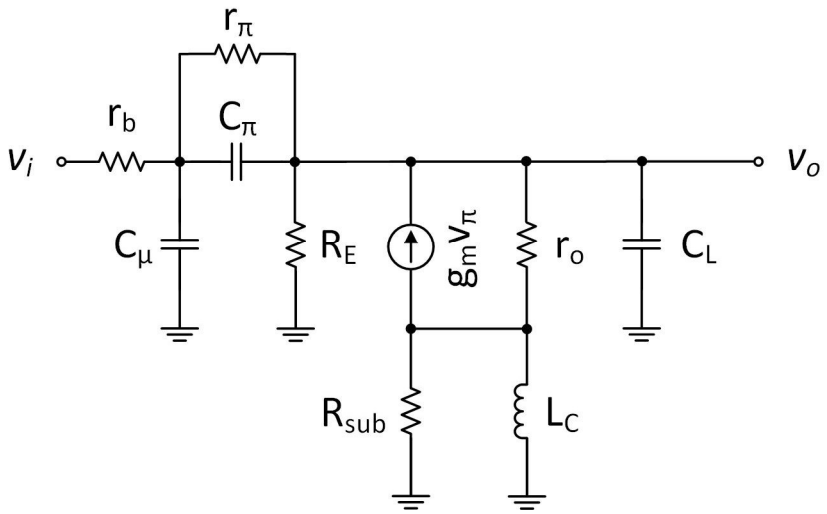
This pole is found by zero-value time constant analysis. The dominant pole in this circuit is related to the load capacitor. Thus the resistance R_L seen by C_L is the same as the output resistance of the emitter follower.

$$\omega_p = \frac{1}{\frac{r_b + r_\pi}{\beta_0 + 1} C_L} \tag{4-3}$$

The zero has the effect of bringing the output of the circuit to 0, therefore it needs to be considered what could prevent the input from reaching the output. Figure 4-2 shows two zeros of the circuit. The first zero occurs if $r_\pi \parallel C_\pi$ shows infinite impedance, thus it blocks the signal from input to output. The second zero occurs if $R_{sub} \parallel L_C$ gives infinite impedance, thus it blocks the current through the transistor yielding zero output. The first



(a)



(b)

Figure 4-1: *(a) Emitter follower with collector inductor (b) Small-signal equivalent circuit*

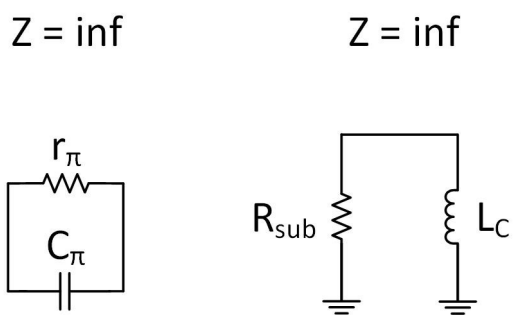


Figure 4-2: *Zeros of the circuit*

zero is hard to be realized because the impedance of $r_\pi \parallel C_\pi$ is small. By selecting proper value of L_C, the impedance of $R_{sub} \parallel L_C$ could be large enough to realize the second zero. If the second zero is dominant, it yields the zero in the low-entropy form of the transfer

function as shown in Equation 4-4.

$$\omega_z = \frac{R_{sub}}{L_C} \tag{4-4}$$

The transfer function in the low-entropy form is expressed in Equation 4-5.

$$H(s) = \frac{g_m R_E}{1 + g_m R_E} \frac{1 + s\frac{L_C}{R_{sub}}}{1 + s\frac{r_b + r_\pi}{\beta_0 + 1} C_L} \tag{4-5}$$

Figure 4-3(a) shows frequency response of the emitter follower with different capacitive load without collector inductor. It shows that the bandwidth of the emitter follower increases when the load capacitor reduces. Figure 4-3(b) shows the emitter follower with fixed capacitor of 50 fF but different values of collector inductor. It is noticed that the bandwidth is extended, however the proper value of the inductor should be selected otherwise the peaking effect would be too large.

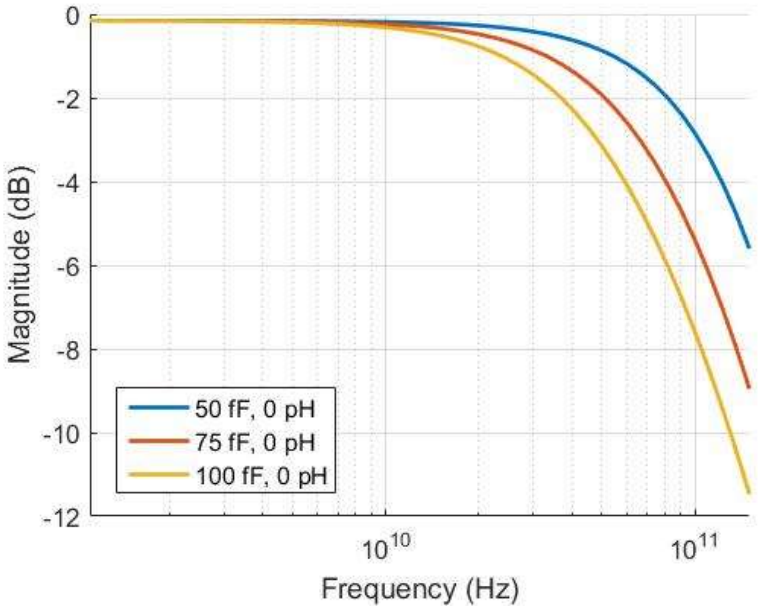
Figure 4-4 shows the comparison between the frequency response of the modeling and simulation result. If the modeled capacitor is used as 50 fF, the frequency response without collector inductor would be almost same as the simulated results. There is some deviation between the model and simulation. To obtain a similar peaking effect, the collector inductor is increased around 3 times compared to parameter in the simulation. The mismatch between the modeling and simulation shows the drawback of the FACTs. Since this method ignores non-critical factors and uses the simplified model, therefore peaking effect caused by the zero is compensated or smoothed by other factors. FACTs give only the direction of the design but not concret design parameter, which can only be obtained from the simulation.

4.2 Schematic Analysis and Design

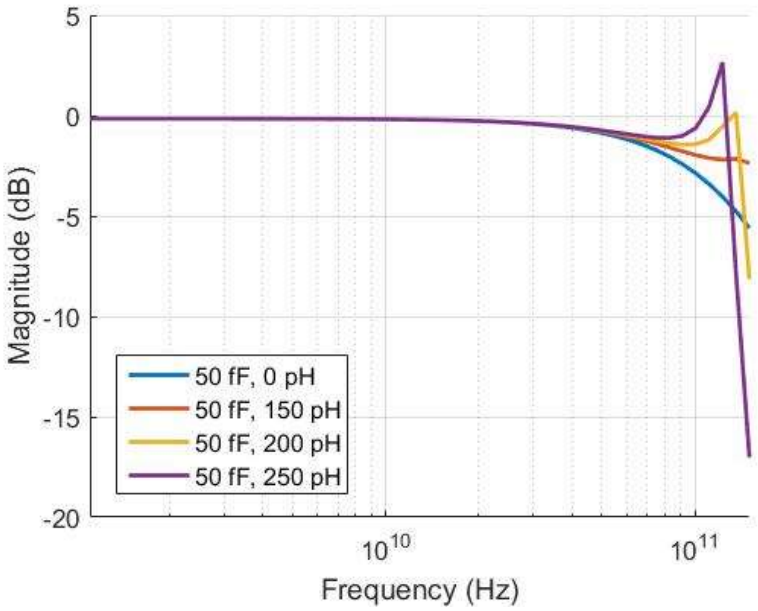
The core schematic of the THA is shown in Figure 4-5. The core circuit operates fully differential with a differential signal input (in+, in-), differential clock input (track, hold, track_d, hold_d), and differential signal output (out+, out-). All the high-frequency ports are connected to on-chip microstrip transmission lines and are terminated with 50 Ω resistors near the transistors to ensure the impedance matching.

The input stage is realized with a differential cascode amplifier $Q_{1,2,3,4}$ with the size of 140/900 nm. The collector resistor R_c of the differential amplifier is used as pull-down resistor to control the base voltage of the SEF Q_9. The size of Q_9 is 140/900 nm, R_C is set to 100 Ω and R_E is 60 Ω. The cascode topology, the peaking capacitor C_E, and peaking inductor L_P of the emitter follower are used to increase the input bandwidth. C_E is set to 80 fF. The size of the hold capacitor C_H is 30 fF to achieve higher bandwidth. $Q_{7,8}$ with the size of 140/900 are the switches of the SEF controlled by the differential clock signal (track, hold).

The small size of the hold capacitor aggravates the problem of signal feedthrough during the hold mode. The capacitor C_{FT} constructed by four transistors with the size of 140/900 nm is cross-coupled to the input and output of the differential SEFs, thus reducing the feedthrough during hold mode [36]. To further increase the feedthrough isolation, $Q_{5,6}$



(a)



(b)

Figure 4-3: *Frequency response of the emitter follower with (a) various capacitive load (b) various collector inductor*

(140/900 nm) are used to control the tail current of the input buffer. During hold mode, the input buffer is switched off and the tail current lowers the base voltage of Q_9 through R_C and $Q_{10,11}$. $Q_{10,11}$ have the size of 140/900 nm. Another benefit of $Q_{5,6}$ is that it reduces the demand of the pull-down voltage on R_C. Usually this voltage is selected to be relatively large in order to turn off Q_9. Since the input buffer is already disabled in the hold mode, the pull-down voltage does not have to be very large, which reduces the size of $Q_{7,8,9}$ and R_C. The clock control of $Q_{5,6}$ is the delayed clock track_d and hold_d. The

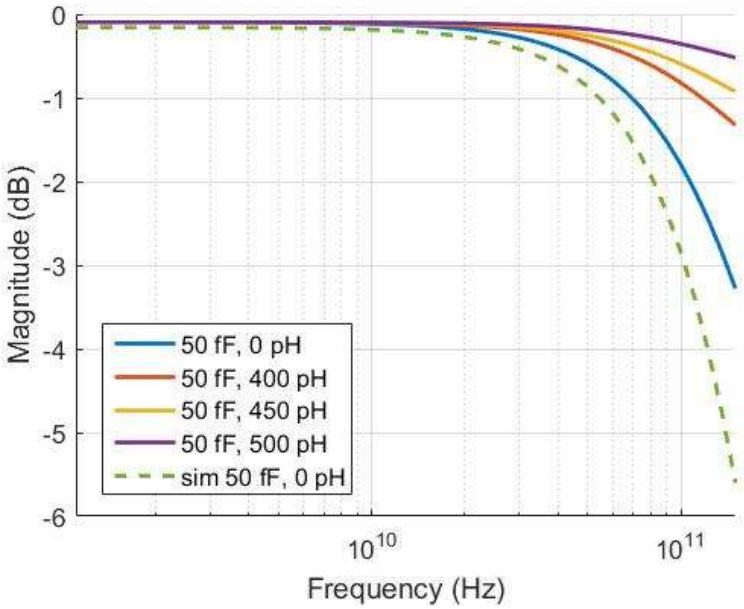


Figure 4-4: *Comparison between the frequency response of the modeling and simulation result for 50 fF hold capacitance and various inductance values*

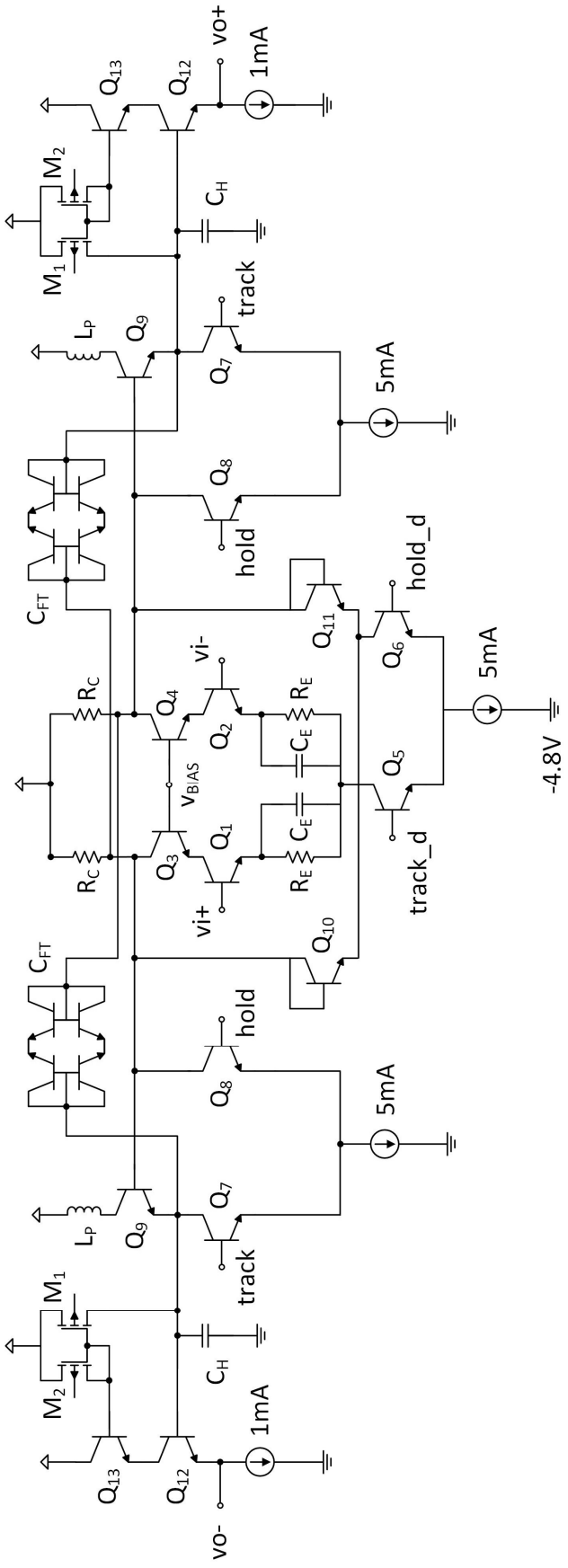


Figure 4-5: *Schematic of SEF based THA with buffer*

delay ensures that the sampled value is not influenced by the switching of the tail current. It is generated from an extra amplifier after the differential clock (track, hold), which adds 3 ps delay according to simulation.

The emitter followers Q_{12} represent input buffers to the 50 Ω output buffer. The size of Q_{12} is 70/900 nm, it is small to reduce the leakage current in the hold capacitor. The base current of Q_{13} with the size of 70/900 nm is compensated through a PMOS current mirror $M_{1,2}$ to further reduce the droop [44]. The size of M_1 is 2.5/1 um and M_2 is 1/1 um.

4.2.1 Power Consumption

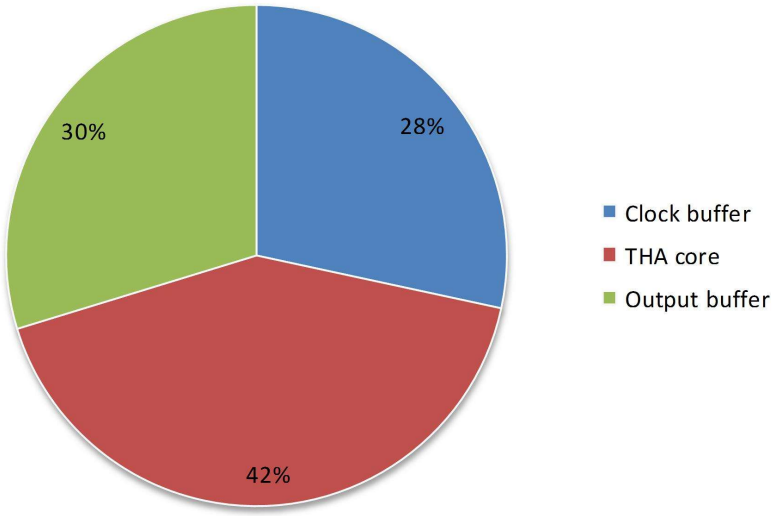


Figure 4-6: *Power consumption breakdown chart.*

The power supply was chosen to -4.8 V, the current consumption is 78 mA, thus the DC power is 375 mW. The power consumption breakdown chart is shown in Figure 4-6. The high power consumption is due to two reasons. The first reason is that there are CML switches used to control the circuit operation mode while generally bipolar CML is power hungry. The second reason is due to the fact that higher current through a differential amplifier brings more linearity and bandwidth. Also more voltage is needed between VCC and VEE to design differential cascoded amplifier with emitter degeneration, which also yields more linearity and bandwidth. Therefore the supply voltage -4.8 V had to be relatively large.

4.3 Layout and Chip

The layout of the THA core with input, output and clock buffers is shown in Figure 4-7. The main components of the design are marked in the figure. All differential high-speed circuitry was designed perfectly symmetric and as compact as possible. The active area including the inductance is only 180 x 190 um^2. The peaking inductance for the SEF was implemented by using an octagonal differential inductor with a center tap connected to the supply.

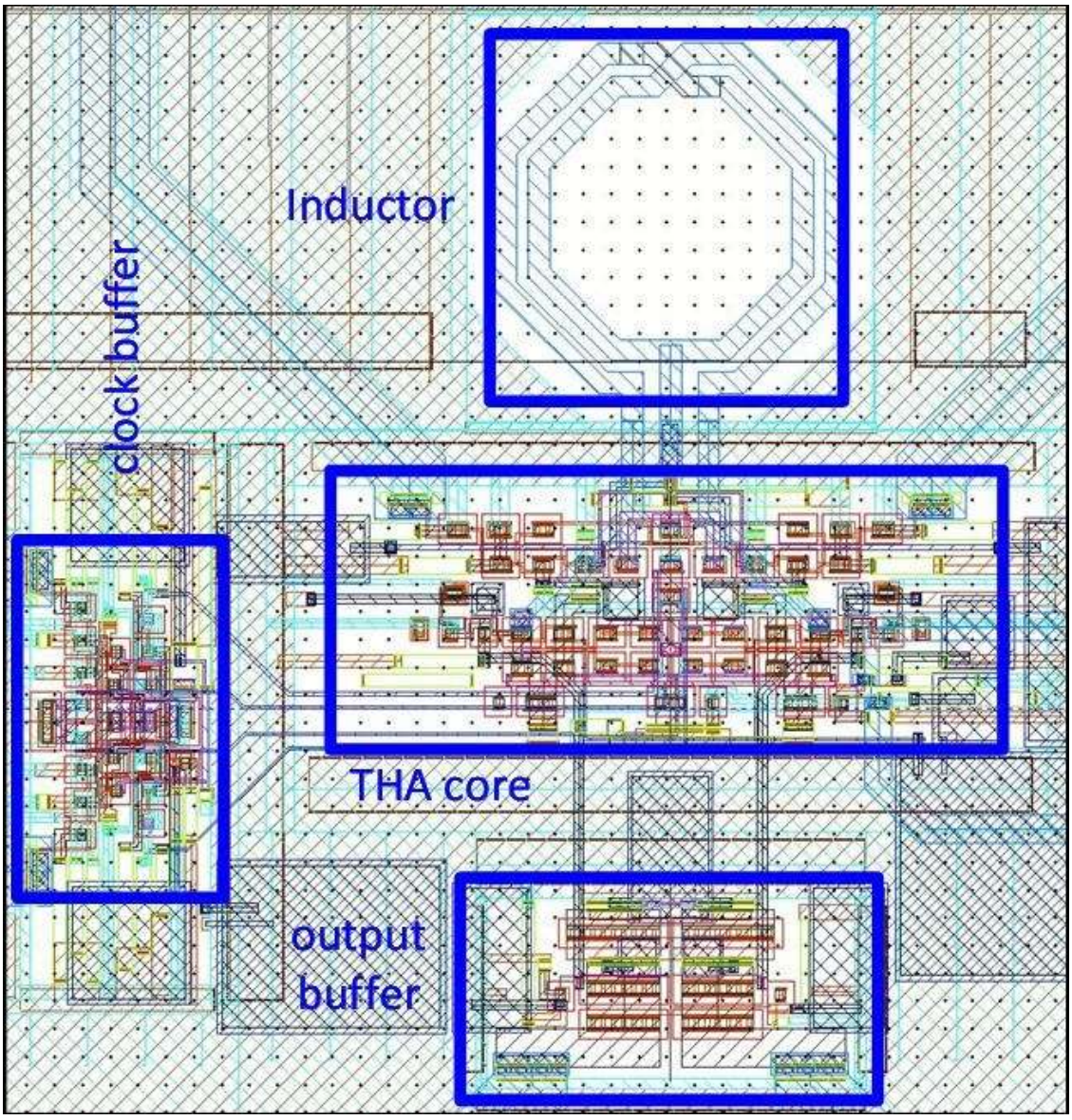


Figure 4-7: *Layout of THA core with buffer*

The chip was fabricated in a 130 nm SiGe BiCMOS technology from IHP (SG13G2) featuring high-speed Silicon Germanium heterobipolar transistors with cut-off frequencies of f_T/f_{max} = 300/500 GHz [40]. Figure 4-8 shows the micro-photograph of the chip. The total chip size is 0.72 mm^2. The GSGSG pads at the upper and lower side are used for probing input and output signal respectively. The differential clock signal for track and hold at right side is probed with GSSG pads. The on-chip microstrip transmission lines are separated sufficiently to avoid coupling which allows to achieve simultanteous even- and odd-mode impedance matching. The DC pads are located at the chip corners.

4.4 Measurement Results

The measurement is done in both frequency domain (S-parameters) and time domain. The input and output GSGSG pads on the chip are contacted with Infinity probes. In

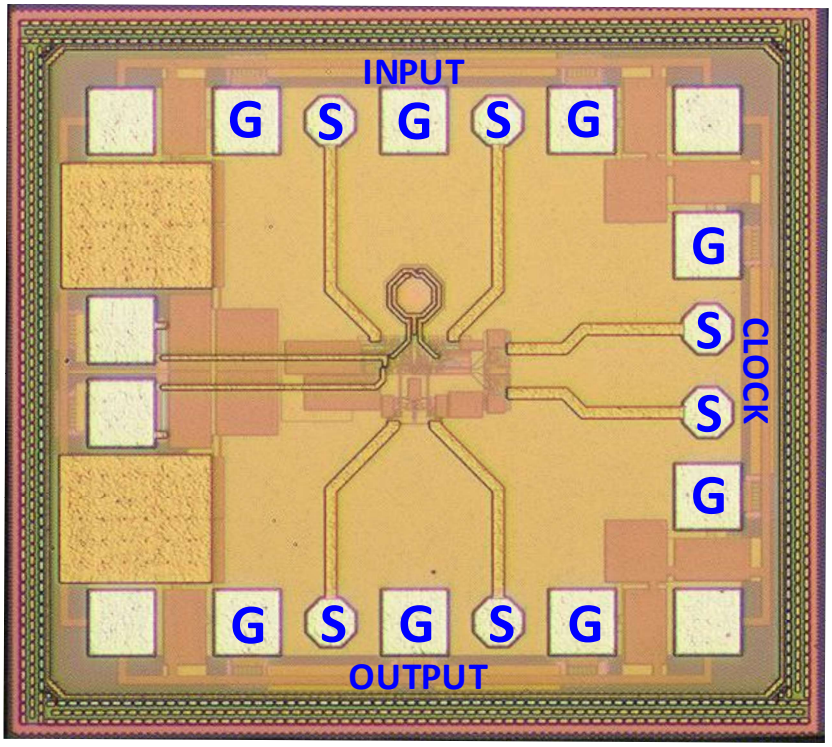


Figure 4-8: *THA chip micro-photograph*

frequency domain, the chip was measured with a static sampling clock signal separately for hold mode and track mode to obtain track mode bandwidth and hold mode feed-through. In time domain, the chip was measured with a sampling oscilloscope and a spectrum analyzer. Different sampling rates were tested. The input frequency extends from 1 to 70 GHz.

4.4.1 RF Module

The RF module is shown in Figure 4-9. The PCB is made from an Isola Tera substrate which was mounted onto a copper plate. The chip was placed into a cavity in the substrate to keep the bond wires between chip and substrate as short as possible. The positive and negative clock signal were able to being wire-bonded to a microstrip transmission line. All RF inputs, outputs, and clock signals are terminated on-chip with 50 Ω. The RF differential input and output signals were not bonded. For these signals on-chip probing was applied.

4.4.2 Test Setup

The test setup for transient and spectrum measurement is shown in Figure 4-10. The main test equipment in this setup is the signal generator 1 (SG1, Keysight E8257D), the PLLs (Linear DC1795A [41], TI LMX2594EVM [42]), the spectrum analyzer (Anritsu MS2760A), and the sampling oscilloscope (Keysight 86100D DCA-X). All signal gen-

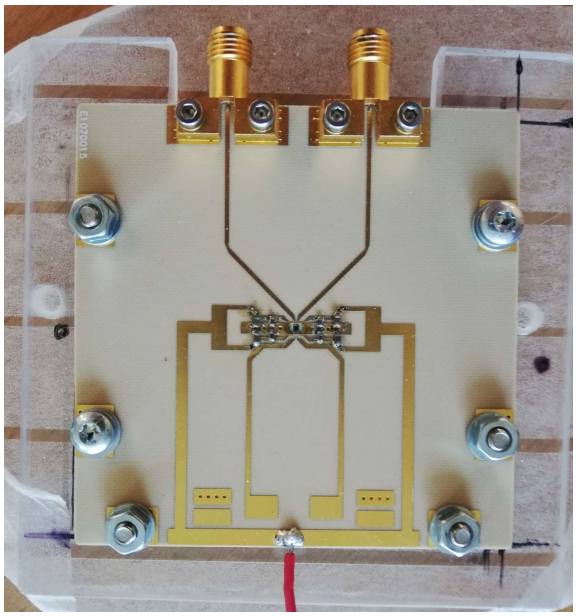


Figure 4-9: *RF module.*

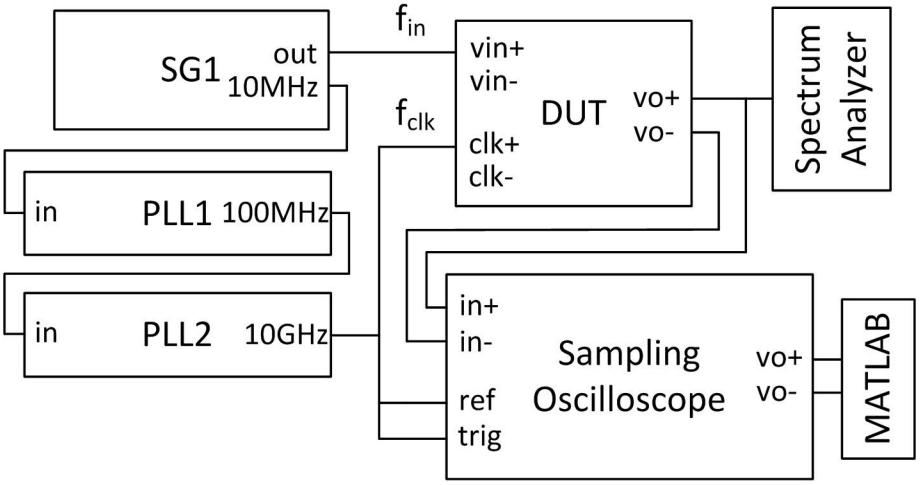


Figure 4-10: *Test setup for transient and spectrum measurement*

erators and the PLLs are synchronized to each other. SG1 is used to generate the input signal for the device under test (DUT, THA), PLLs generates the sampling clock for the DUT. The sampling oscilloscope digitizes the output of the DUT. The output of the PLL provides low phase noise programmable high-frequency trigger clock to the sampling oscilloscope.

It is very similar to the test setup in Figure 3-15. The difference are that PLLs and SG1 are used directly for the clock signal and the baluns are removed. The reason is that relative low sampling rate was applied therefore SG2 is no longer needed and for a wide bandwidth range, the balun causes extra common-mode signal generation due to phase mismatch.

4.4.3 S-Parameter Measurement

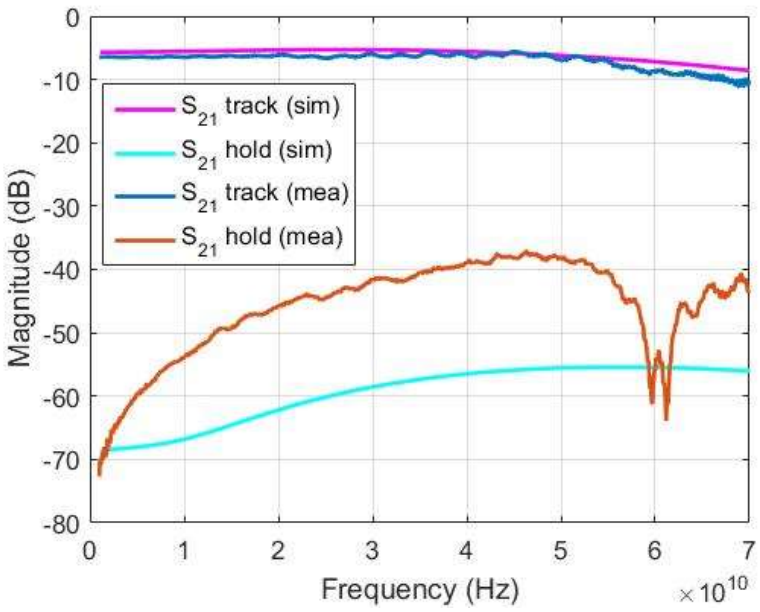


Figure 4-11: *S-parameter measurement results of the THA chip*

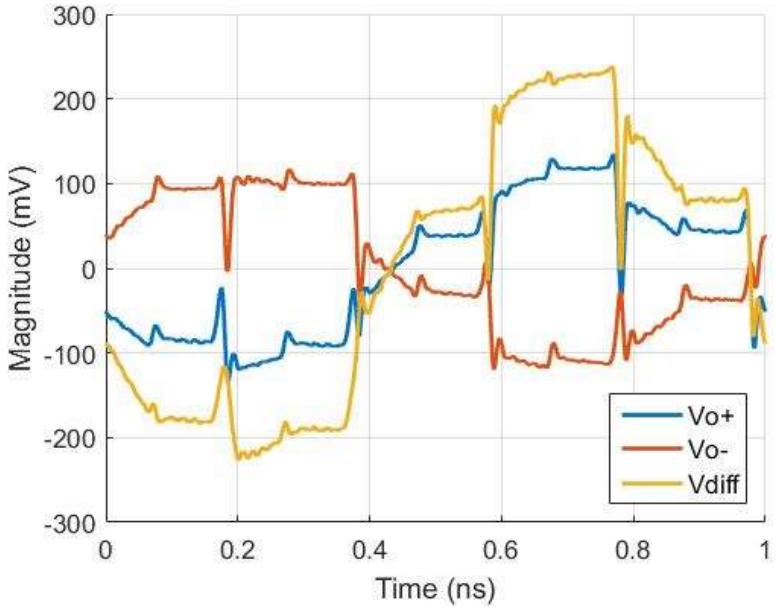
The chip was first tested with a broadband vector signal analyzer (VNA, Anritsu VNA MS4647b) to measure the small signal performance in track and hold mode separately. The test setup is shown in Figure 2-15. Figure 4-11 shows the single-ended post-layout simulation and measurement results from 1 to 70 GHz.

For both input and output, one of the two differential ports was terminated with a 50 Ω resistor, therefore single-ended measurements were performed. The chip is set either in track mode or hold mode using a static clock signal. The gain of the S_{21} in track mode is -6 dB, thus the chip gives unity gain in the differential mode. The 3dB cut off frequency is around 65 GHz indicating very high bandwidth. The S_{21} in hold mode gives at least -38 dB attenuation indicating excellent hold mode feedthrough suppression.

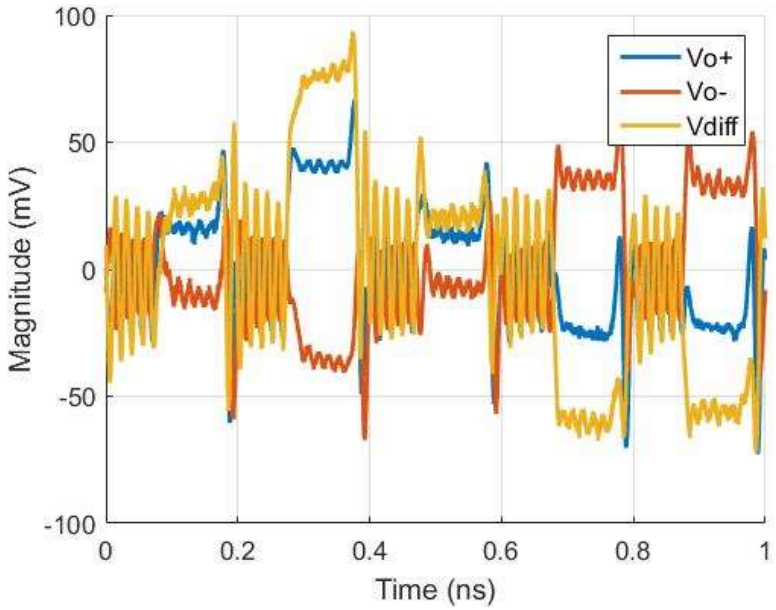
4.4.4 Transient and Spectrum Measurement

Figure 4-13 shows the differential output signal with the frequency of 1 GHz and 61 GHz and 5 GS/s sampling clock. The figure shows the raw data of the positive and negative output signal from the oscilloscope. The differential output is calculated with MATLAB. With this sampling rate, the signal performance during the hold mode is shown very clearly. Figure 4-13 shows the differential output signal with the frequency of 1 GHz and 61 GHz and 10 GS/s sampling clock. Although this chip can still work with 20 GS/s sampling rate the quality of the hold signal becomes somewhat degraded, therefore best results are obtained up to sampling rates of around 10 GS/s.

The single ended output of 1 GHz and 61 GHz input sampled at 10 GS/s measured with the spectrum is shown in Figure 4-14. The test setup is shown in Figure 4-10. The frequency span is the corresponding Nyquist zone of 5 GHz, the resolution bandwidth of



(a)

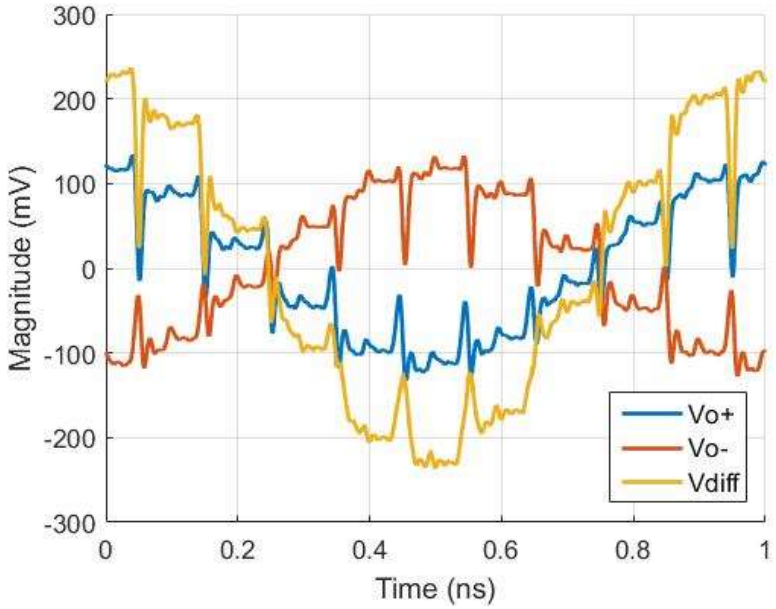


(b)

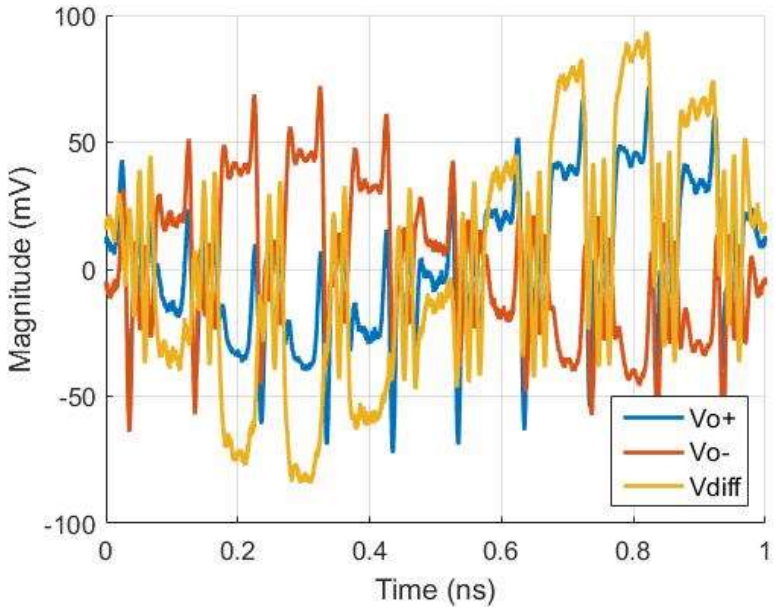
Figure 4-12: *Measured differential output signal with (a) 1 GHz (b) 61 GHz input frequency sampled by 5 GS/s clock*

the spectrum analyzer is 10 kHz. Considering cable loss of around -9.5 dB, the spectrum indicates a 3dB large-signal bandwidth of 61 GHz.

Figure 4-15 shows SFDR, SNDR and THD vs. frequency at 10 GS/s sampling rate. The SFDR reduces with increasing frequency. The best case THD is at 29 GHz with -44 dB, while SFDR is 49 dBc and SNDR-related ENOB is 7 bit. The worst SFDR is 31 dBc at 9 GHz corresponding to an ENOB of 5 bit. The ENOB is larger than 5 bit within the analog bandwidth of the THA from 0 Hz to 61 GHz.



(a)

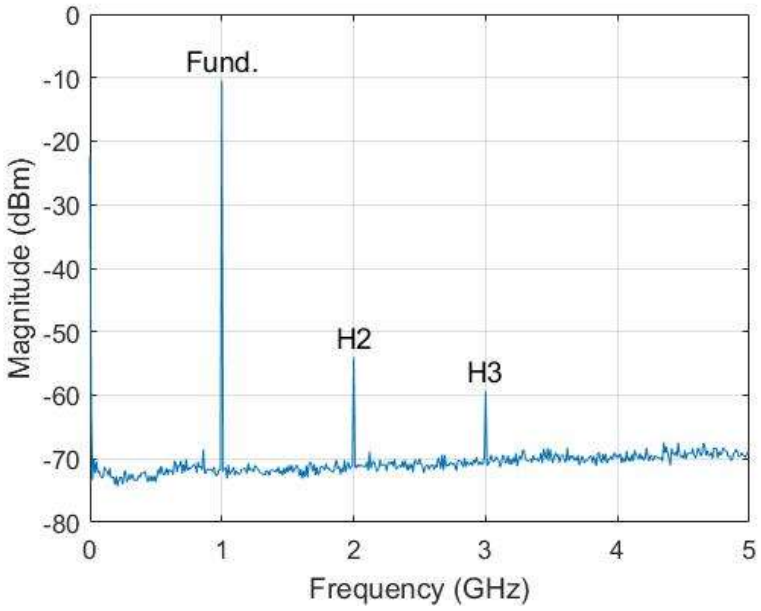


(b)

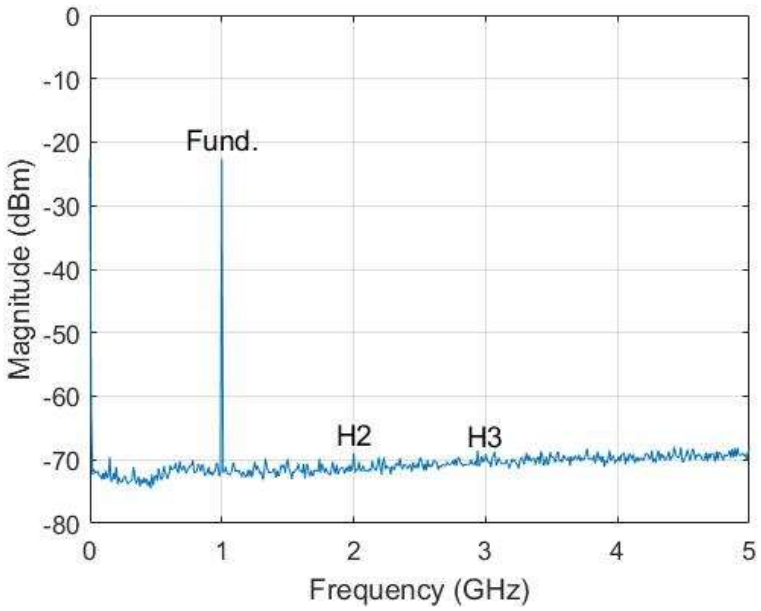
Figure 4-13: *Measured differential output signal with (a) 1 GHz (b) 61 GHz input frequency sampled by 10 GS/s clock*

4.5 Conclusion

This paper presents a differential SEF THA using 130 nm SiGe BiCMOS technology [A2]. The preliminary consideration of bandwidth extension on the emitter follower is discussed. The detailed measurement setup for large-signal measurement is introduced. Both large- and small-signal 3dB bandwidth of the THA reach more than 60 GHz, achieving 61 and 65 GHz bandwidth, respectively. The comparison of this chip to the state of



(a)



(b)

Figure 4-14: *Spectrum of single-ended output signal of (a) 1 GHz (b) 61 GHz single-ended input sampled by 10 GS/s clock*

the art of sampling circuits is shown in Table 4-1. Sampling the input signal at 10 GS/s yields a peak SNDR-related ENOB of 7 bit at 34 GHz. Moreover, this THA achieves an ENOB of at least 5 bit from 1 GHz to 61 GHz, which is better than any THA published so far. The chosen SEF THA topology as well as careful RF optimization of schematic and layout allowed to achieve excellent performance with respect to bandwidth, hold-mode feedthrough, and linearity.

Table 4-1: *Comparison to the state of the art.*

	[31]	[32]	[27]	[A1]	[A2]
Architecture	SEF	Switched capacitor	Charge sampling	SEF	SEF
Input amplitude	160 mVpp	800 mVpp	500 mVpp	450 mVpp	450 mVpp
Max. sampling rate	108 GS/s	25 GS/s	25.6 GS/s	40 GS/s	10 GS/s
Small-signal BW	40 GHz (3dB)	70 GHz (3dB)	N/A	70 GHz (3dB)	65 GHz (3dB)
Large-signal BW	N/A	55 GHz (3dB)	40 GHz (1dB)	19 GHz (3dB)	61 GHz (3dB)
THD@f_{in}	-49dB@1GHz	-39dB@21GHz	-44dB@1GHz	-47dB@1GHz	-44dB@29GHz
ENOB@f_{in}	N/A	4.9@3GHz	6.4@1GHz	7.5@1GHz	7@29GHz
Power	87 mW	73 mW	913 mW	440 mW	375 mW
FoMw	N/A	98 fJ/conv.-step	422 fJ/conv.-step	61 fJ/conv.-step	293 fJ/conv.-step
FoMs	N/A	150 dB	147 dB	153 dB	156 dB
Die area	0.49 mm^2	0.53 mm^2	1.5 mm^2	0.79 mm^2	0.72 mm^2
Process	55 nm SiGe BiCMOS	28 nm CMOS	130 nm SiGe BiCMOS	130 nm SiGe BiCMOS	130 nm SiGe BiCMOS

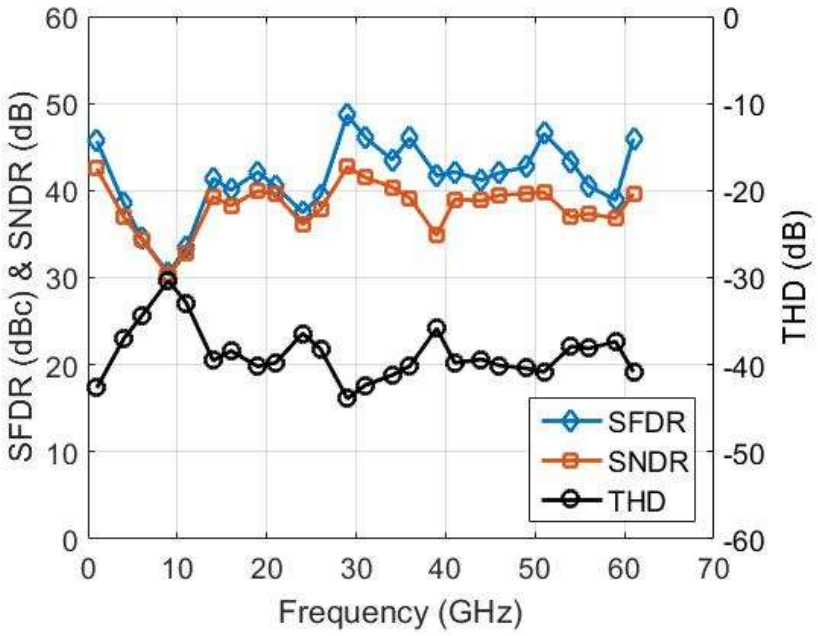


Figure 4-15: *SFDR, SNDR, THD vs. input frequency by 10 GS/s clock*

5 Design, Realization, and Measurement of an STI Sampler

In this chapter a novel STI sampler chip is presented. The concept of STI sampling is introduced in Chapter 2.2.

5.1 Architectures of STI Sampler

5.1.1 Conventional Architectures of STI IHC with Single Delay Element

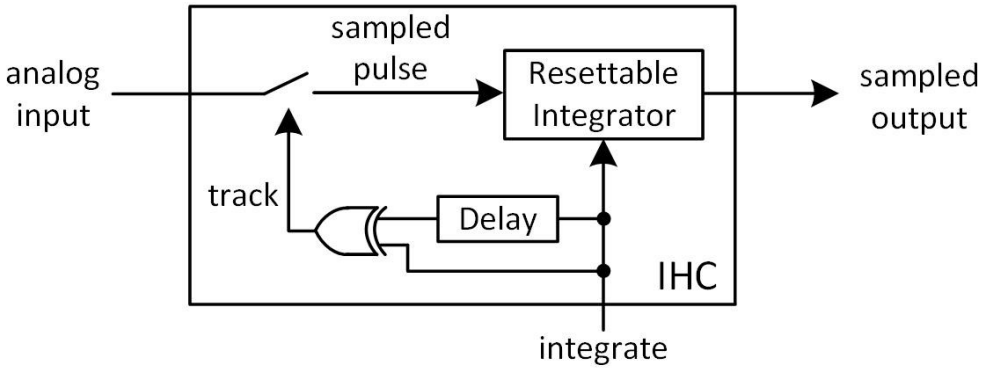
The core element of an STI sampler is the IHC. Figure 5-1(a) shows a straightforward way using a single delay element to realize the STI IHC. The track signal is generated from the integrate signal with delay element and XOR gate. The delay is equal to the integrate duration. As shown in Figure 5-1(b), the structure generates a track pulse synchronized with integrate and reset. This topology generates in total two pulses. The width of the sampled pulse is the same as the width of the track pulse. The pulse width depends on the rise and fall time of the switch. Therefore even if the delay can be made very small, it is still very challenging to design the ultra-fast switch.

Figure 5-2(a) shows another solution using less components. In this structure, the sampled pulse is not generated directly. Instead, it uses the time delay between track and integrate, which is generated by the delay element. The integrator integrates the tail part of the track signal, thus only the falling edge is integrated. The reason is that if peaking technique is used to increase the bandwidth, the rising edge of the track signal will have distortion, therefore the tail part would be a better choice to be sampled.

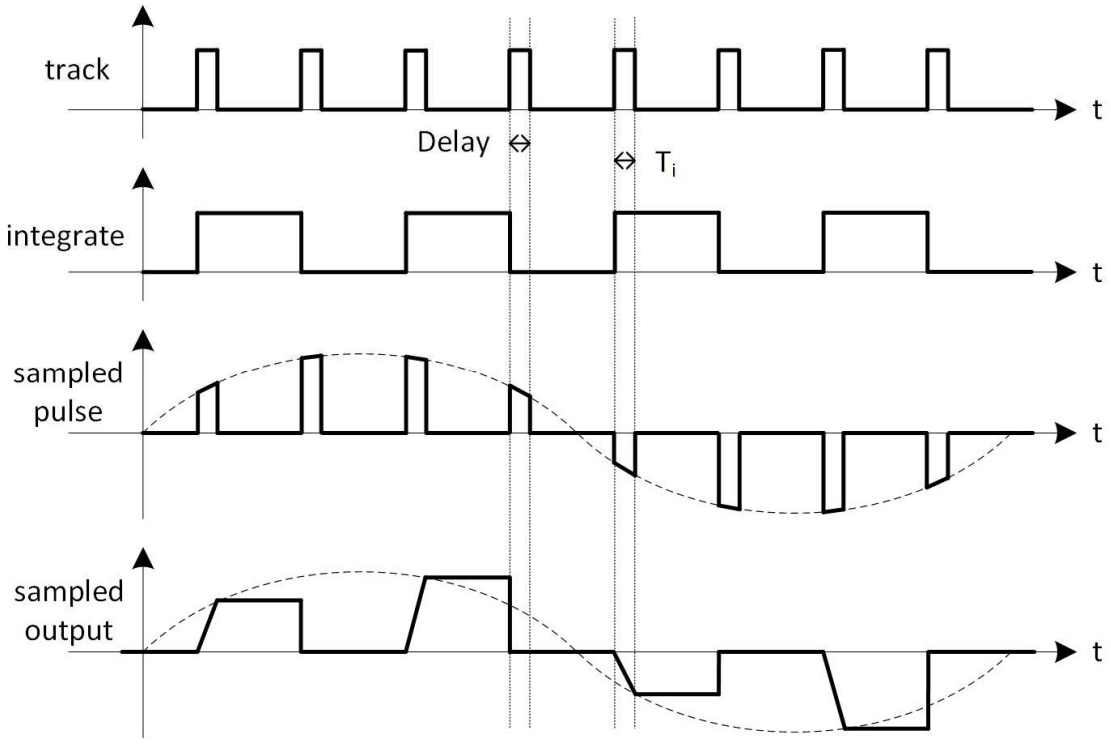
The potential issues of these two structures are the design limitation of the delay element and the non-perfect hold state. The single delay element has its minimum delay and tunable range. This limits the bandwidth of the IHC due to bandwidth being proportional to $1/T_i$. The key point to have perfect hold state is a perfectly zero input for the integrator. However, when the switch turns off, the signal needs some settling time to finally reach zero and tends to exhibit ringing. This ringing effect causes the degradation of the hold signal.

5.1.2 Novel Architecture of STI IHC with Differential Delay Scheme

The bandwidth of STI sampler is highly depending on the integration time. The shorter the integration time of the STI sampler is, the higher is it's bandwidth. As shown in the previous paragraph for a bandwidth of higher than 50 GHz a pulse width of less than 10 ps is needed which is very difficult to achieve because it would require extreme low signal rise and fall times. Furthermore, it must be ensured that the switch is completely switched from off-state to on-state and then back to off-state again in such a short time. Hence to achieve the highest possible bandwidth for our STI IHC we propose a new architecture using two switches and a differential delay scheme as shown in Figure 5-3. The main

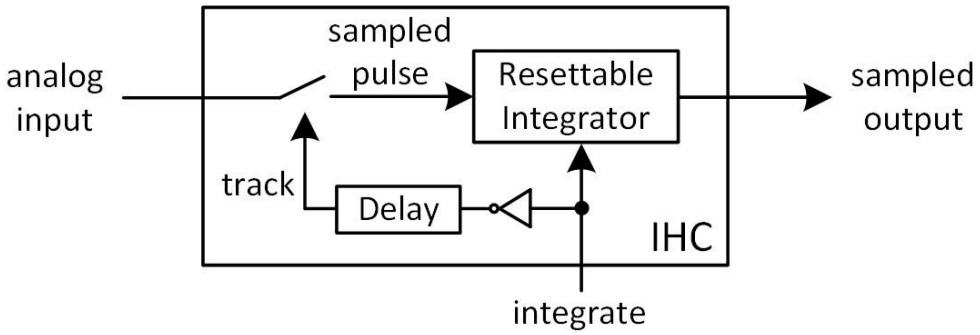


(a)

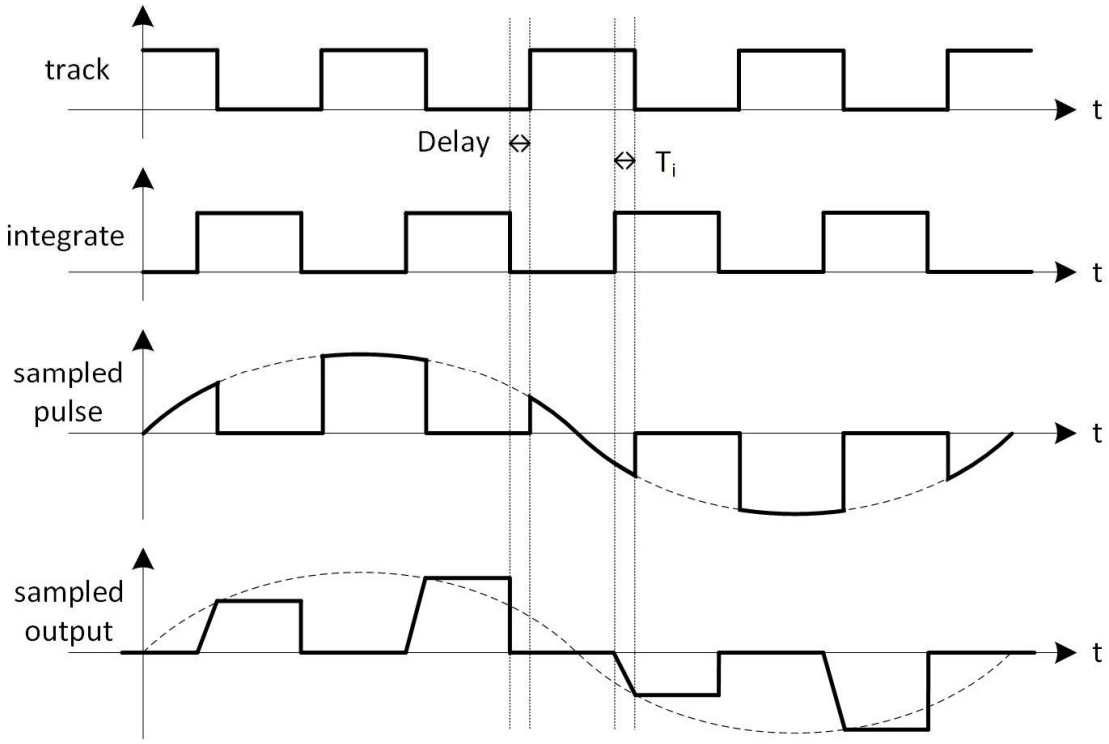


(b)

Figure 5-1: *(a) STI IHC using single delay and XOR gate. (b) Input, output, and control signals.*

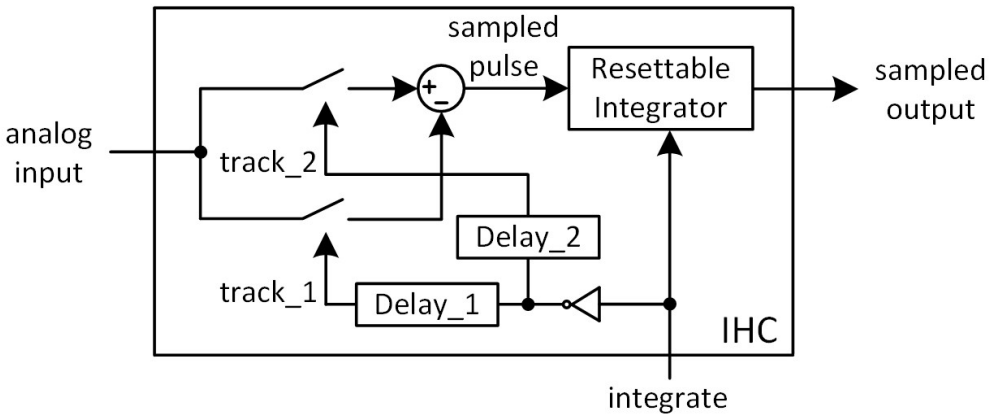


(a)

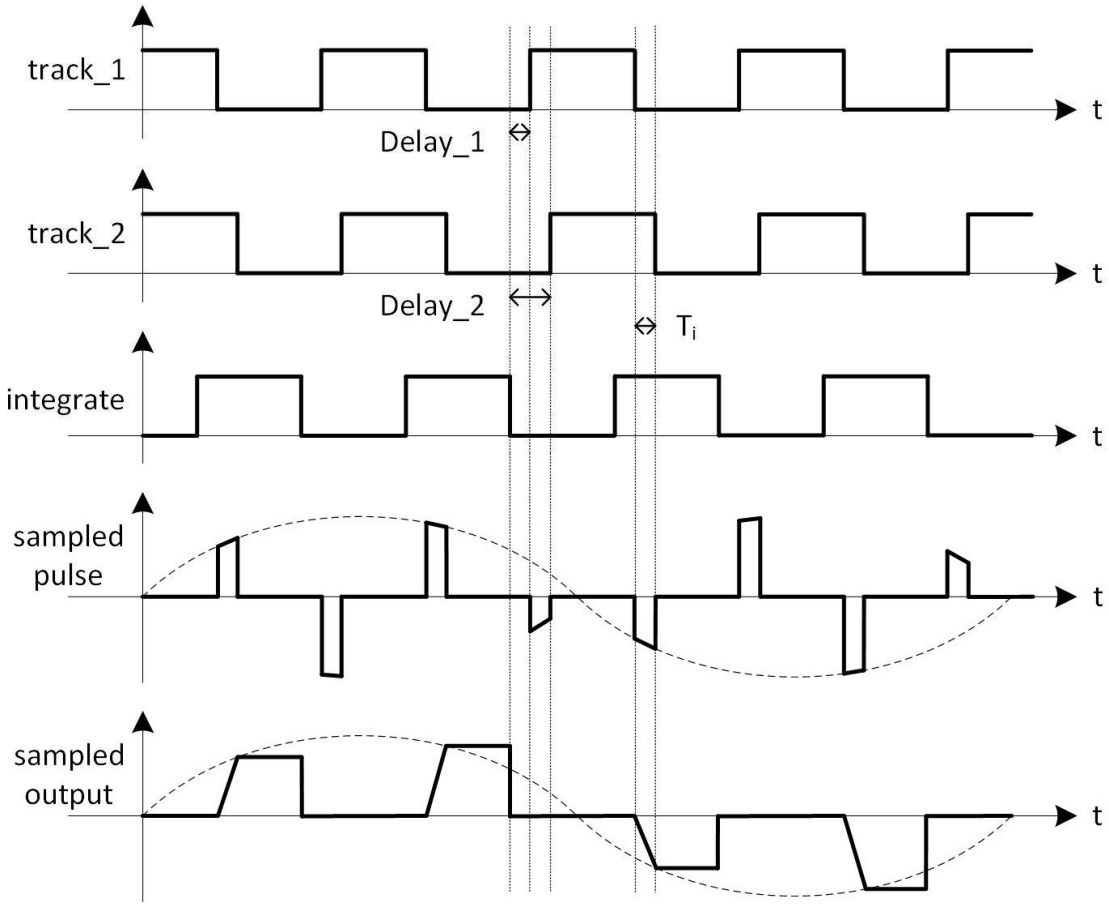


(b)

Figure 5-2: *(a) STI IHC using single delay. (b) Input, output, and control signals.*



(a)



(b)

Figure 5-3: *(a) STI IHC using differential delay. (b) Input, output, and control signals.*

components are two switches, one subtractor, two tunable delays, an inverter, and a resettable integrator. The control signals are integrate, track_1, and track_2, where the track signals are the inverse of integrate signal delayed by the tunable delay elements Delay_1 and Delay_2. The delay difference generated from the two different delays determines the integration time T_i, and thus sets the bandwidth of the sampler. The delay difference between two tunable delay elements can be made very short, therefore very high bandwidth can be achieved using this delay scheme. The subtraction of the output signals of the two switches sets the input signal of the integrator to 0 after T_i. Hence the subtractor has to generate very short pulses and must be carefully optimized for maximum bandwidth. Alternatively the subtractor can be omitted if an integrator with a differential input is used. In this case slew-rate and high-frequency common-mode suppression of the integrator must be carefully optimized.

Another advantage of the differential scheme with two track signals is that their non-ideal pulse shapes can be compensated to some extent if the shapes of the falling signal edges of the output signals of the two switches are made equal. Ideally, to obtain a perfect hold signal the input signal should be precisely zero for the integrator in the hold state. However, when the switches turn off, the output signal of the switch needs some settling time and it also shows some ringing before reaching zero. Ringing is especially a problem if the track signal exhibits an ultra-short fall time. However if the output signals of both switches exhibit similar shapes for the falling edge, the effect of the imprecise switching is compensated by subtraction at the input of the integrator. Hence with the differential delay scheme and symmetric switching behavior of the two switches the precision of the sampling can be greatly increased.

5.2 System Analysis of STI Sampler

5.2.1 STI Sampling with Non-zero Rise and Fall Time

Sampler precision suffers from various non-idealities which is especially true for broadband samplers. For example the performance of conventional broadband sampling circuits is significantly degraded by the rise time of the sampling clock which increases the aperture time [45]. A similar problem exists in STI samplers where the non-zero rise and fall times of the track signal (cf. Figure 2-8) degrade the desired rectangular pulse shape of the track signal to a more trapezoidal or triangular type of shape. The effect of non-zero rise and fall time on the pulse shape and the sampled pulse is depicted in Figure 5-4.

Figure 5-4(a) depicts three pulse shapes, a rectangular, a triangular, and a Gaussian pulse shape. The pulse shapes can be understood as window functions by which the input signal is weighted before it is integrated by the IHC. In the ideal case, the sampling window represents a rectangular pulse. A more realistic window function approximates the track pulse as a trapezoidal pulse with the parameters pulse width T_i, rise time t_{rise}, and fall time t_{fall}. If $T_i = (t_{rise} + t_{fall}) / 2$, the trapezoidal pulse becomes a triangular pulse (see Figure 5-4(a)). An even more realistic pulse shape is given by the Gaussion pulse shape shown in the same Figure.

For triangular and gaussian pulse, the width of T_i is the full width at half maximum (FWHM). The standard deviation σ of the gaussian pulse is equal to $T_i/2.355$. The math-

ematical expression of ideal and non-ideal STI sampling using different window functions W_τ are shown in Equation (5-1).

$$
\begin{aligned}
v_o(t) &= \frac{1}{T_i}\int_{-\infty}^{+\infty} v_{in}(\tau)\cdot W(\tau)\,d\tau \\
W_{rec}(\tau) &= \begin{cases} 1 & t \le \tau \le t+T_i \\ 0 & \text{others} \end{cases} \\
W_{tri}(\tau) &= \begin{cases} \tau/T_i & t \le \tau \le t+T_i \\ -\tau/T_i & t+T_i \le \tau \le t+2T_i \\ 0 & \text{others} \end{cases} \\
W_{gau}(\tau) &= \begin{cases} \frac{1}{\sqrt{2\pi}\sigma} e^{-\frac{t^2}{2\sigma^2}}, T_i = 2.355\sigma & t \le \tau \le t+2T_i \\ 0 & \text{others} \end{cases}
\end{aligned}
\tag{5-1}
$$

The Fourier transform of W_{tri} is the Fourier transform of W_{rec} to the power of 2, i.e. a squared *sinc* function. The transfer function of the non-ideal triangular pulse sampling is given in Equation (5-2), it is a square of the ideal transfer function. The Fourier transform of W_{gau} is also a gaussian function. The transfer function of the gaussian pulse sampling is given in Equation (5-3).

The comparison of the STI sampler bandwidth due to different pulse shapes but equal T_i is shown in Figure 5-5 whereby the frequency is normalized to the 3dB cut-off frequency of the ideal STI sampler. Signal weighting with triangular and Gaussian pulses exhibits a very similar frequency response. In these cases the bandwidth of the non-ideal STI sampler is reduced by 30% compared to the ideal case.

$$
|H_{STI,tri}(\omega)| = \left(\frac{\sin(\omega\frac{T_i}{2})}{\omega\frac{T_i}{2}}\right)^2 = |H_{STI}(\omega)|^2. \tag{5-2}
$$

$$
|H_{STI,gau}(\omega)| = e^{-0.5\omega^2(T_i/2.355)^2} \tag{5-3}
$$

5.2.2 IHC with Integration Capacitor Leakage

Figure 5-6 shows the gain-frequency performance for an ideal integrator and an integrator with integration capacitor leakage. The ideal integrator exhibits an infinite DC gain which is physically impossible to realize. In reality an electronic integrator exhibits a finite DC gain which is caused by the finite output resistance of output transistors and leakage current in the integration capacitor [20]. These effects shift the pole from 0 Hz to ω_H as shown in Figure 5-6.

At lower frequencies, the gain difference between the ideal and nonideal integrator is large. At high frequencies the gain of the transistors drop which causes a second pole. This pole can be shifted to frequencies beyond 100 GHz using fast transistors of advanced semiconductor technologies as will be shown in section IV. Therefore the second pole is

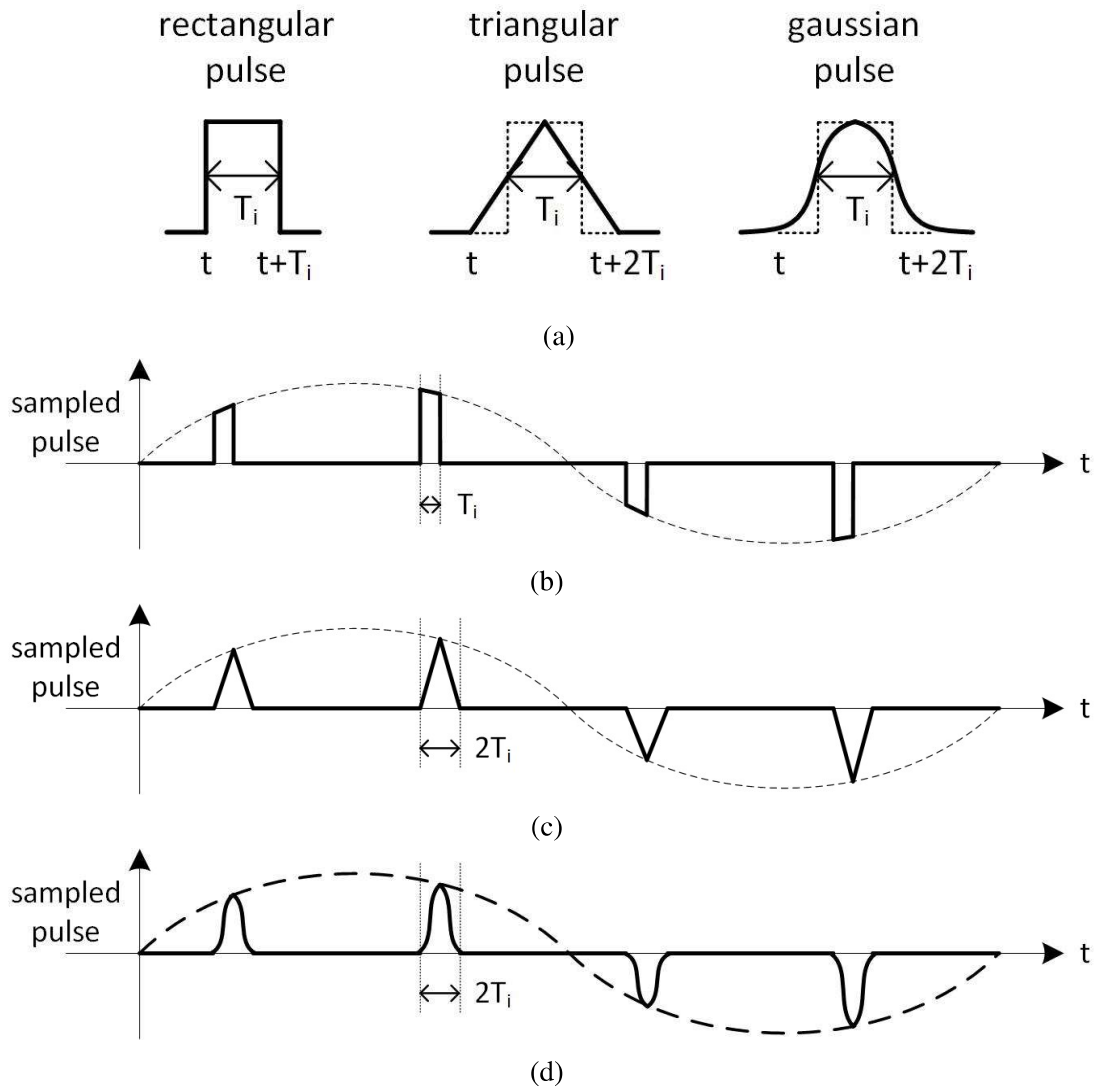


Figure 5-4: *(a) Ideal and non-ideal sampling window (b) Rectangular pulse sampled output (c) Triangular pulse sampled output (d) Gaussian pulse sampled output.*

not shown in Figure 5-6. The bandwidth of the nonideal integrator is ω_H, the unity gain (0dB) bandwidth is ω_T. For both ideal and nonideal integrator the gain-bandwidth product is $\frac{1}{T_i}$, and the parameters of their frequency responses can be related to each other by

$$\omega_T = \omega_H \cdot A_{DC,nonid} = \frac{1}{T_i} = A_i. \tag{5-4}$$

In each sampling period the integrator is reset. Hence for the calculation of the error induced by the non-ideal integrator only a single pulse needs to be considered at the input of the integrator. In addition, we assume that if the pulse width T_i is small enough, there is little difference if an RF signal or a DC signal is applied to the input of the IHC. Therefore the input signal can be approximated by a flat rectangular pulse. Assuming an infinite slew rate, only the amplitude of the pulse signal influences the integration error. The worst case of the voltage error due to limited DC gain of the integrator occurs for maximum pulse amplitude, i.e. for a pulse amplitude equal to full-scale voltage V_{FS} of the ADC.

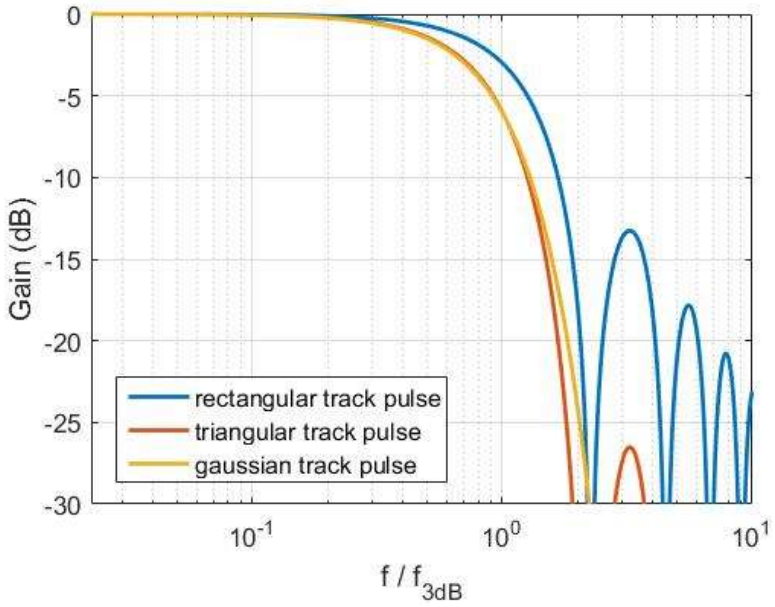


Figure 5-5: *Bandwidth comparison of STI sampling with rectangular, triangular and gaussian track pulses.*

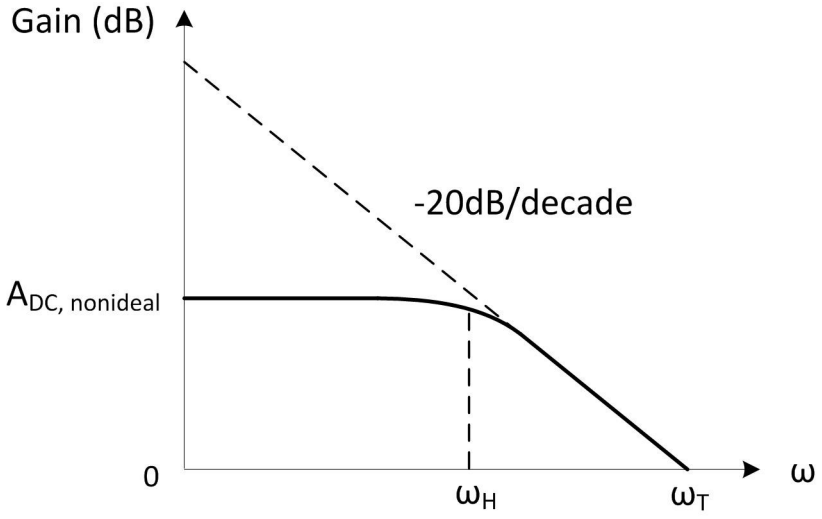


Figure 5-6: *Frequency response of ideal and non-ideal integrator.*

Figure 5-7 shows the voltage error caused by the non-ideal integrator. The reset phase is not shown here. The non-ideal integrator will cause a voltage error for both the integrate and hold phase. The non-ideal integrator works as a low-pass filter, the step response of the IHC in the time domain is given by

$$\begin{aligned} v_o &= A_{DC,nonid} \cdot v_{in}(1 - e^{-\frac{t}{\tau}}) \\ &= A_{DC,nonid} \cdot v_{in}(1 - e^{-T_i\omega_H}) \\ &= A_{DC,nonid} \cdot v_{in}(1 - e^{-1/A_{DC,nonid}}) \end{aligned} \tag{5-5}$$

where $\tau = \frac{1}{\omega_H}$ and $t = T_i$. The gain factor $A_{DC,nonid}(1 - e^{-1/A_{DC,nonid}})$ is closer to 1 if $A_{DC,nonid}$ is larger. Assume the full scale is V_{FS}, the integrate error of the maximum DC input

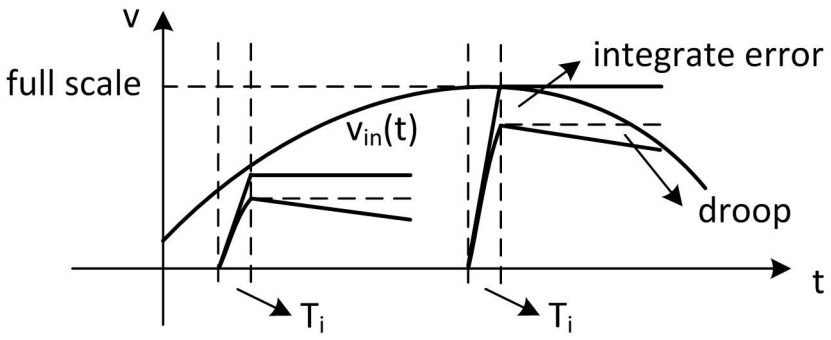


Figure 5-7: *Voltage error caused by the nonideal integrator.*

yields

$$\begin{aligned} v_{int\_err} &= V_{FS} - v_o \\ &= V_{FS} \cdot (1 - A_{DC,nonid}(1 - e^{-1/A_{DC,nonid}})). \end{aligned} \tag{5-6}$$

The droop is calculated as follows,

$$v_{droop} = v_o - v_o e^{-t\omega_H} = v_o - v_o e^{-T_h\omega_H} \tag{5-7}$$

where T_h is the duration of the hold state. The voltage error based on the integrate error and droop, yields

$$v_{err} = v_{int\_err} + v_{droop} \tag{5-8}$$

Assume the duration of the hold state is k times the integration time, thus $T_h = k \cdot T_i$, yields

$$\begin{aligned} v_{err} = V_{FS} \cdot (1 - A_{DC,nonid} \cdot (1 - e^{-1/A_{DC,nonid}}) \\ \cdot e^{-k/A_{DC,nonid}}) \end{aligned} \tag{5-9}$$

The voltage error should be less than the LSB of the N bit ADC so that v_{err} has to be

$$v_{err} < V_{LSB} = \frac{1}{2^N} \cdot V_{FS}. \tag{5-10}$$

Equation (5-9) and (5-10) allow to estimate the effect of integrator leakage on the ADC resolution and to optimize it such that it does not degrade ADC resolution.

As an example, assume if V_{FS} is 1 V and $A_{DC,nonid}$ is 500 (54 dB), the voltage error is 0.0109 V while the integration error is much smaller than 0.0001, hence the droop dominates the voltage error. The least significant bit (LSB) of a 5-bit ADC is $\frac{1}{2^6} = 0.0156$. Therefore with a DC gain of 50dB the voltage error would be smaller than the LSB of the ADC.

The previous calculation focused only on the influence of $A_{DC,nonid}$ on v_{err}. However also offset voltages and currents in the integrator will degrade integration respectively sampling precision. These offset effects might be small because the integrator is reset in each sampling period and they depend strongly on the selected circuit topology of the integrator. In practice offset effects have to be considered as well and, if needed, appropriate offset cancellation or calibration techniques need to be applied.

5.3 Preliminary considerations

5.3.1 Negative Resistance with Cross-coupled Transistors

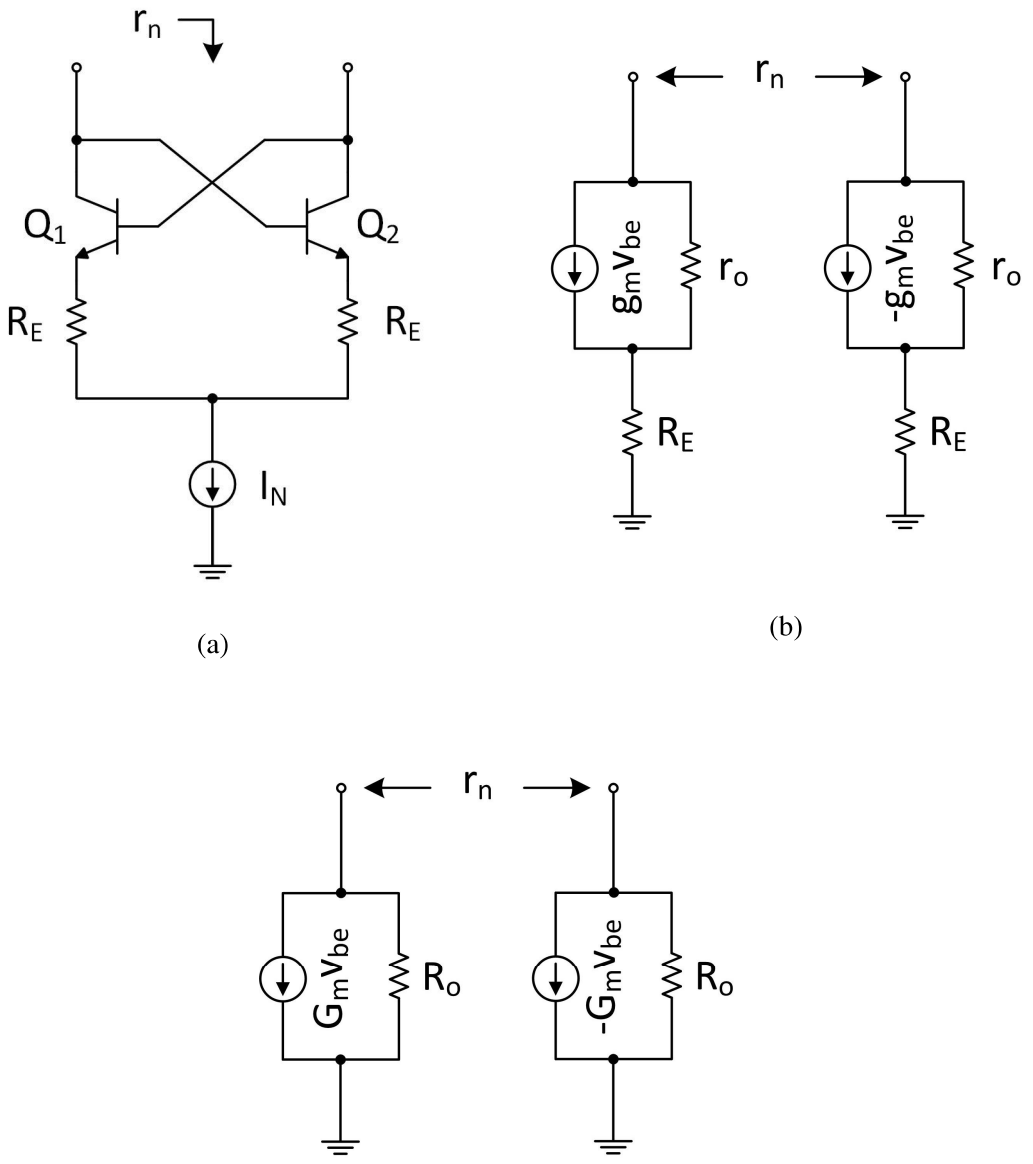


Figure 5-8: *(a) Negative resistance using cross-coupled transistor (b) Small-signal equivalent circuit (c) Small-signal equivalent circuit using the equivalent of emitter degeneration*

The small-signal negative resistance can be realized by multiple ways [46]. One possibility is to use cross-coupled bipolor transistors. Figure 5-8(a) shows the the cross-coupled transistor $Q_{1,2}$ with emitter degeneration resistance R_E, the bias current is I_N. The neg-

ative resistance seen from the collector of two transistor is r_n. Figure 5-8(b) shows the small-signal equivalent circuit of Figure 5-8(a). Figure 5-8(c) uses the equivalent model of emitter degeneration to represent Figure 5-8(b), as mentioned in Chapter 3.1.4.

$$gm = \frac{I_N/2}{V_T} = \frac{qI_N/2}{kT} \tag{5-11}$$

$$G_m \simeq \frac{g_m}{1 + g_m R_E}$$

$$R_o \simeq r_o\,(1 + g_m R_E)$$

$$r_n \simeq -\frac{2}{G_m}(1 + \frac{1}{G_m R_o}) \approx -\frac{2}{G_m} \tag{5-12}$$

Equation (5-12) shows the formula of r_n. G_m is influenced by the emitter degeneration resistance R_E, g_m is influenced by the bias DC current I_N. Therefore I_N and R_E are two extra parameters to modify r_n, besides the size of $Q_{1,2}$, which can also change g_m.

5.3.2 Integrator with Negative Resistance

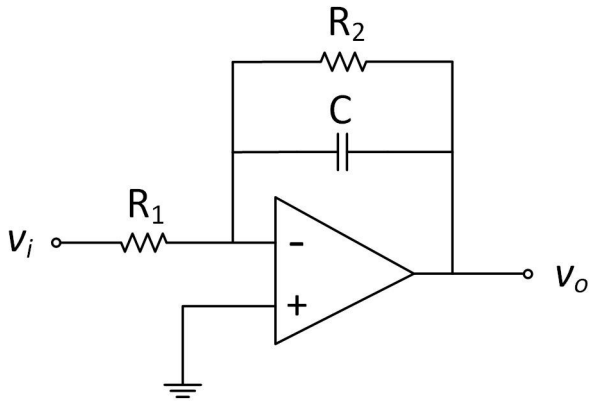


Figure 5-9: *Integrator circuit using operational amplifier*

During the practical design of the integrator, it is usually realized with the operational amplifier. Figure 5-9 shows a typical design of integrator circuit using operational amplifier. Equation (5-13) shows that the DC gain of the integrator is $-\frac{R_2}{R_1}$ and ω_H is equal to $\frac{1}{R_2 C}$. The integrator should have large DC gain and low 3dB bandwidth, which leads to large R_2.

$$H(s) = -\frac{R_2}{R_1}\frac{1}{1 + \frac{s}{\omega_H}} \tag{5-13}$$

$$\omega_H = 2\pi f_H = \frac{1}{R_2 C} \tag{5-14}$$

Figure 5-10 shows one solution to make R_2 large. It uses negative resistance r_n parallel with positive resistance R_C. If the absolute values of their impedances are the same, they

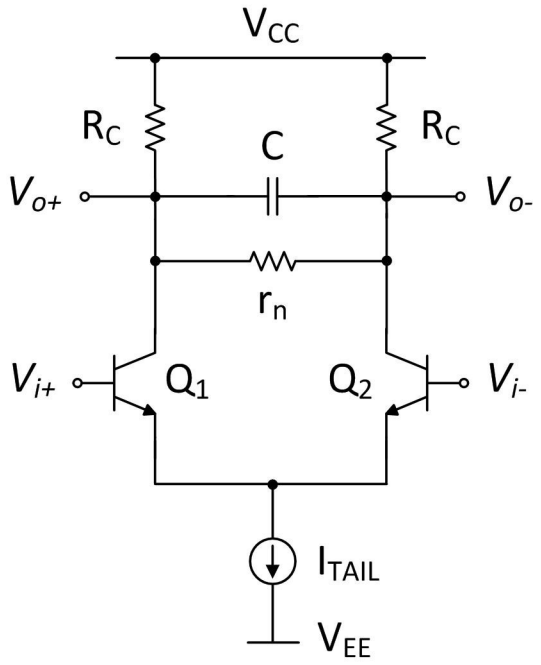


Figure 5-10: *GmC-Integrator with negative resistance*

will create infinite resistance. Equation (5-15) shows the calculation of R_2 from Figure 5-10.

$$R_2 = 2R_C \parallel r_n \tag{5-15}$$

Figure 5-11 shows how voltage across the capacitor with positive or negative resistance changes over time. When the load resistance is positive, the voltage drops, when the load resistance is negative, the voltage increases over time. This result can be very useful for calibrating the integrator in the hold mode. Since R_C is fixed, if $|r_n|$ is smaller than R_C, then R_2 is positive, otherwise R_2 is negative. Therefore checking the performance of the signal in the hold mode can directly calibrate the positive and negative resistance to be the same, yields to near infinite R_2.

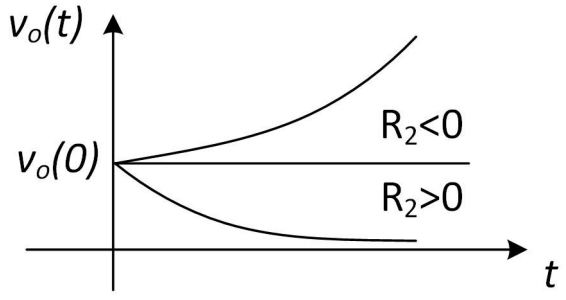


Figure 5-11: *The voltage across the capacitor with positive or negative resistance*

The effect of negative resistance on the hold signal is shown in Figure 5-12. These effects are based on different tail currents of negative resistance. When the tail current is small,

R_2 becomes positive, the hold value reduces. When the tail current is large, R_2 becomes negative, the hold value increases. This feature can be very useful to solve the issue of signal droop.

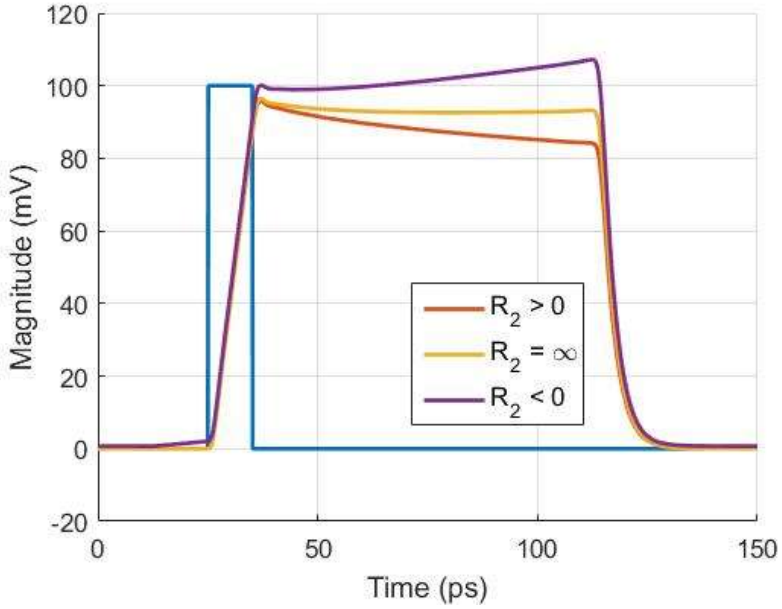


Figure 5-12: *Simulation of the hold signal with positive or negative resistance* R_2

5.4 Schematic Analysis and Design

5.4.1 Tunable Delay Element

The design task of the delay element is to generate delay in the range of around 5 ps tuned by a control voltage. Figure 5-13 shows the schematic of the delay circuit using delay interpolation. This circuit is constructed with three unity gain differential amplifiers Q_1Q_2, Q_3Q_4 and Q_5Q_6. The transistors have the same emitter width/length of 70/900 nm. The differential amplifier Q_3Q_4 is working as a delay element with the tail current of 0.5 mA. R_C is equal to 200 Ω. The other two amplifier are controlled by the current switch Q_7 and Q_8 with the voltage signal V_{BIAS}. The tail current is 2 mA. The third differential amplifier Q_5Q_6 receives the signal from the first amplifier Q_1Q_2 delayed by the second amplifier Q_3Q_4. The signal from Q_1Q_2 and Q_5Q_6 are added together to the output. The delay of the whole circuit is depending on the current switch controlled by the voltage difference X. When X is changing from negative to positive, more delay is added to the output.

Assume that the delay element can provide a delay from $d1$ to $d2$ ps. Using identical tunable delay circuits as shown in Figure 5-14 and setting the delay of *Delay*_1 and *Delay*_2 from $d1$ and $d2$ allows to generate a differential delay between *track*_1 and *track*_2 from 0 to $d1 - d2$.

Figure 5-15 shows simulation results of the tunable delay, *track*_1 and *track*_2 have delay between 0.5 ps and 5 ps by tuning *Delay*_1 and *Delay*_2.

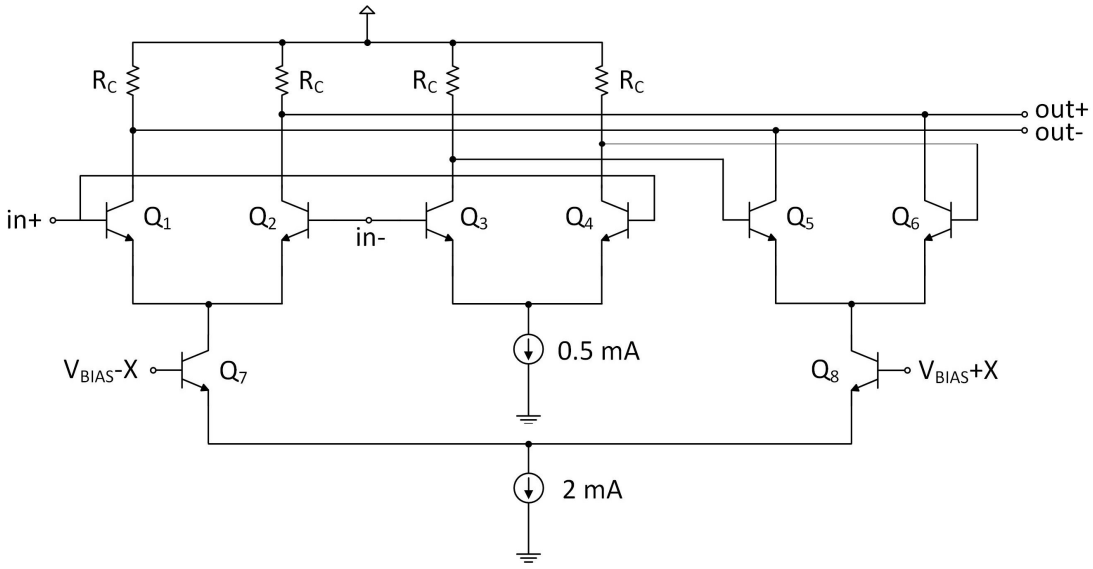


Figure 5-13: *Tunable delay element.*

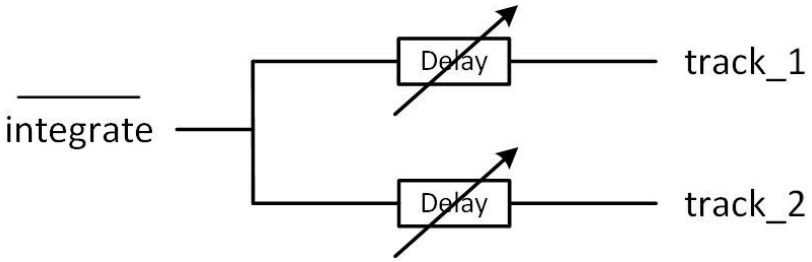


Figure 5-14: *Differential delay elements.*

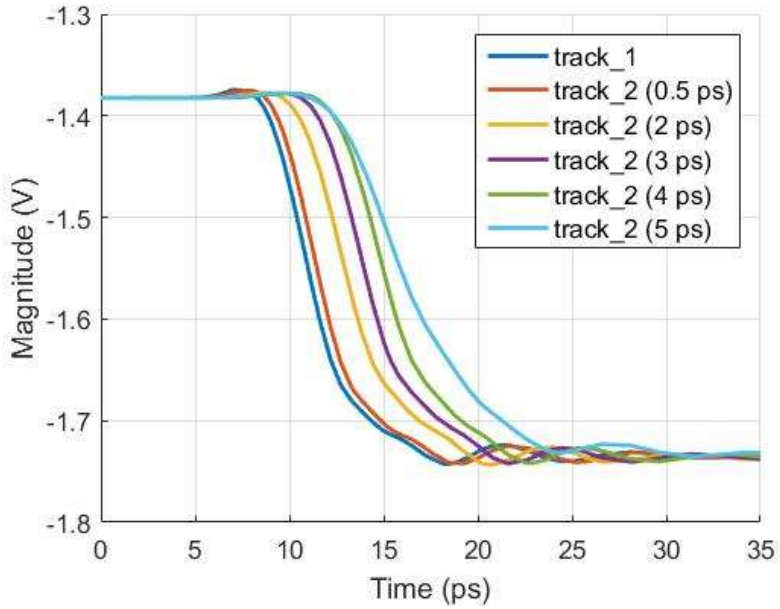


Figure 5-15: *Clock output of different delay.*

We simulated the noise of the delay amplifiers which was less than 0.09 mV RMS and the signal gradient 350 mV / 5 ps. From that we calculated the jitter due to additive noise which resulted in an RMS jitter of less than 1.3 fs. Therefore the additive noise induced jitter in the delay was neglected in the jitter analysis. The detailed jitter analysis was done in Chapter 2.

5.4.2 Differential Current-Mode-Logic Switch

The differential CML switch is working as both switch and input buffer for the integrator. The bandwidth limitation of the STI IHC is supposed to be the integration duration, therefore the switch should have bandwidth over 100 GHz. Figure 5-16 shows the schematic

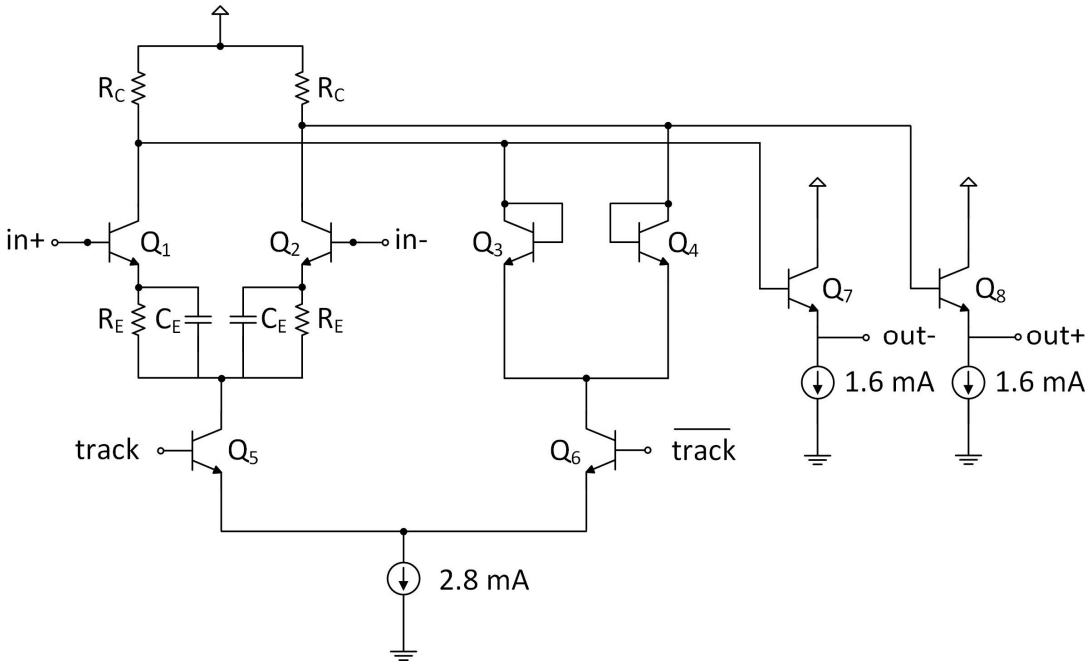


Figure 5-16: *Broadband CML switch.*

of the broadband CML switch. The transistors Q_5Q_6 act as current switches controlled by the clock signal *track* and $\overline{track}$. When *track* is on, the switch is working as a unity gain broadband differential amplifier Q_1Q_2 for the input signal input+ and input-. R_C and R_E are chosen to 400 Ω and 320 Ω, respectively. When $\overline{track}$ is on, the switch will output 0V differential voltage because the voltages over Q_3Q_4 are identical. Two emitter followers Q_7Q_8 are used as buffers for the output signals. A peaking capacitor C_E of 18 fF is used in the differential amplifier Q_1Q_2. The size of the peaking capacitor can be large because the distortion caused by the zero will be compensated by the pole of the integrator. The transistors have the same size of 70/900 nm except Q_5Q_6 which are 140/900 nm.

5.4.3 Subtractor

The topology of the subtractor is the same as that of the adder. As shown in the Figure 5-17, the subtractor consists of two differential amplifiers Q_1Q_2 and Q_3Q_4 with the size

of 210/900 nm, which share the same collector resistors. R_C is set to 100 Ω and R_E to 22 Ω. The difference compared to the adder is that differential inputs of the second differential amplifier Q_3Q_4 have been flipped. Q_7 to Q_{10} construct the cascode amplifiers using common base stages as active loads to increase the bandwidth. Q_5 and Q_6 with the size of 140/900 nm are emitter followers used as output buffer. Figure 5-18 shows the

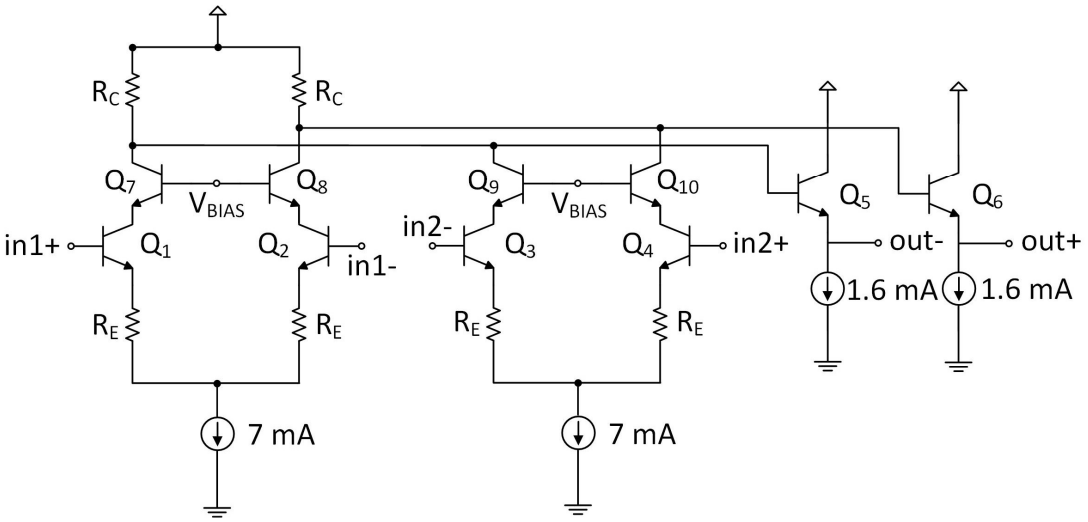


Figure 5-17: *Subtractor.*

simulated output voltage of the subtractor when applying an ideal rectangular pulse with 5 ps pulse width to one of the input of the subtractor. The pulse response of the subtractor converts the rectangular input pulse to pulse with an approximately gaussian pulse shape.

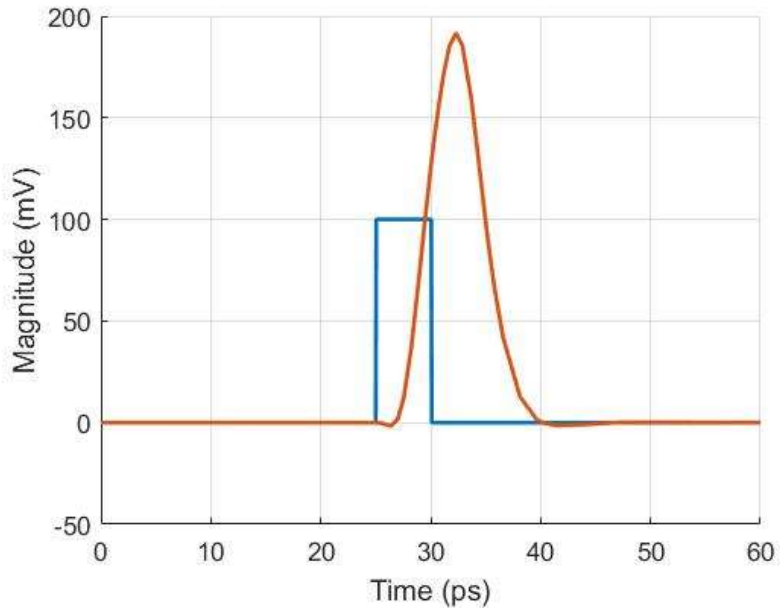


Figure 5-18: *Simulated pulse response of the subtractor.*

5.4.4 High-speed Resettable Integrator

The resettable integrator is the key element in the STI IHC. It should offer a high DC gain and unity gain bandwidth. Furthermore, IHC linearity should be good, i.e. the integrator should achieve a sufficiently large linear range at DC and neglectable slew-rating. [47] presented an ultrabroadband NPN-only integrator using a differential negative resistance in parallel to collector resistors to achieve a large integrator DC gain. The integrator in this paper uses a similar topology to realize the IHC. Figure 5-19 shows the

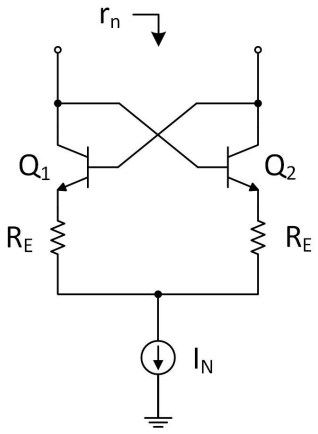


Figure 5-19: *Negative resistance with cross-coupled transistor.*

cross-coupled transistor $Q_{1,2}$ with emitter degeneration resistors R_E, the bias current is I_N. The differential small-signal negative resistance r_n seen into the collectors of the two transistors is given by

$$r_n \simeq -2 \cdot \frac{1 + g_m R_E}{g_m} \tag{5-16}$$

In the IHC design I_N and R_E were optimized to maximize the DC gain of the IHC. It should be noted that after fabrication the DC gain of the IHC can be tuned by adapting I_N. The DC gain of the IHC should be maximized as it influences the sampling precision both in integrate mode and hold mode. Hence by tuning I_N the influence of process, supply voltage, and temperature tolerances on the precision of the IHC can be compensated.

The schematic of the resettable integrator is shown in Figure 5-20. The design of the integrator is based on the differential amplifier Q_1Q_2 with emitter lengths/widths of 280/900 nm, R_C (200Ω) and R_E (20Ω). The resettable integrator has two states, integrate and reset, which are realized by varying load impedances in parallel to the differential load capacitance C_{INT} and load resistance $2R_C$. The varying load impedances are realized by the negative resistance of Q_3Q_4, and R_N and the differential diode pair Q_5Q_6. The differential amplifier and its loads are controlled by the signals *integrate* and $\overline{integrate}$ using the current switches Q_7Q_8 and Q_9Q_{10}. Q_7Q_8 are 350/900nm, Q_9Q_{10} are 140/900 nm. When *integrate* is on, Q_1Q_2 see a very high load resistance. The near infinite resistance is achieved by setting the negative resistance generated by the cross-coupled transistor pair Q_3Q_4 to -$2R_C$. R_N and DC current I_N both determine the negative resistance. R_N is set to 135 Ω and Q_3Q_4 to 70/900 nm while I_N is tunable. When $\overline{integrate}$ is on, the diode pair

Q_5Q_6 with the size of 280/900 nm is switched on to achieve a small differential load resistance and zero differential voltage over the integration capacitor C_{INT} in order to quickly discharge C_{INT}. C_{INT} is set to 120 fF.

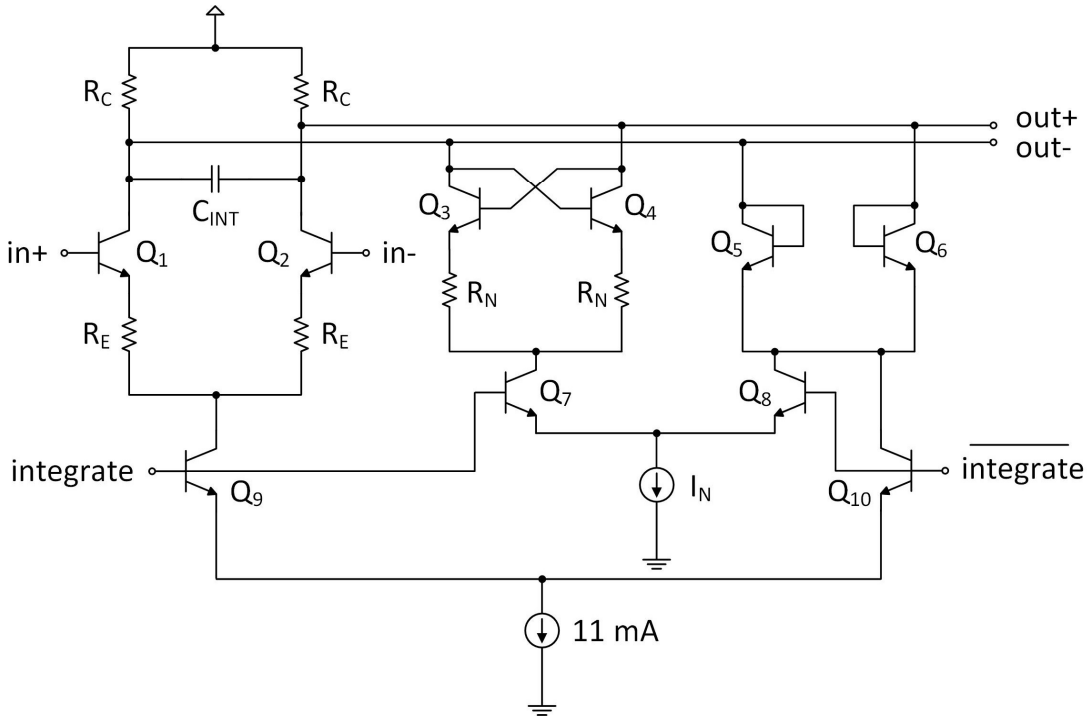


Figure 5-20: *Resettable integrator.*

Figure 5-21 shows the frequency response of the integrator. The capacitor value of 120 fF results into an ω_T of 8 GHz and a DC gain of 60 dB. The equivalent T_i is around 20 ps based on Equation (5-4), which is not sufficient if a unity-gain sampler is the design target. Therefore an amplifier is needed after the integrator. The calculated error based on Equation (5-9) is 0.0027, which is smaller than the LSB of an 8-bit ADC.

The harmonics of the sampled signal depend on the DC linearity and the slew rate of the integrator. Figure 5-22 shows the linear range of the integrator of around 500 mVpp. V_{in} is the voltage difference between *in+* and *in−*, where *in−* is constant and *in+* is swept in the DC analysis . V_{out} is the voltage difference between *out+* and *out−*. In the DC analysis, the capacitor becomes an open circuit, thus the DC linearity of the integrator represents the combined linearity of the differential amplifier (Q_1,Q_2, R_C) and the negative resistance (Q_3,Q_4, R_N).

The slew rate of the integrator is simulated by applying an ideal rectangular pulse with 10 ps pulse width and different magnitudes to the input of the integrator as shown in Figure 5-23(a). The ratio between the hold signal voltage and the input pulse amplitude should be constant. However it reduces when the input magnitude becomes larger, thus reducing the linearity of the output signal as shown in Figure 5-23(b). The range with neglectable slew rate is approximately as large as the low frequency linear range. This can be understood from the fact that the integrator is starting to slew rate when the input transistors are no longer operating in small-signal region.

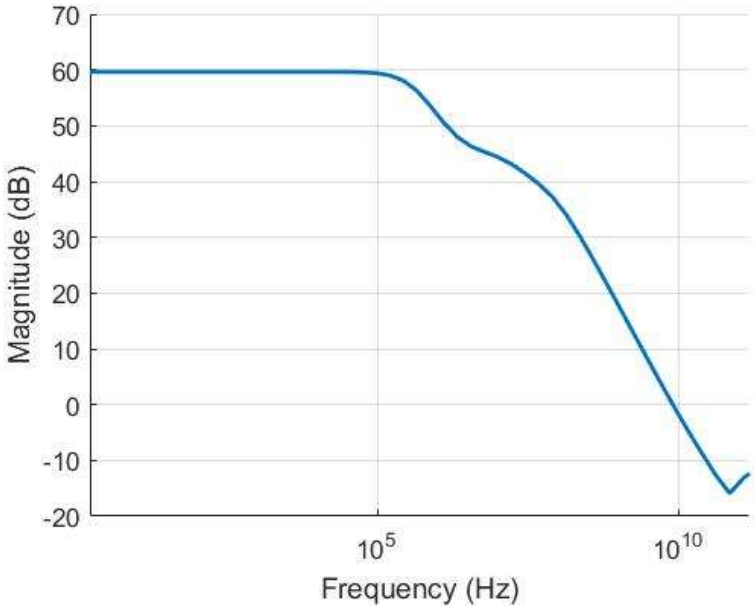


Figure 5-21: *Frequency response of the integrator.*

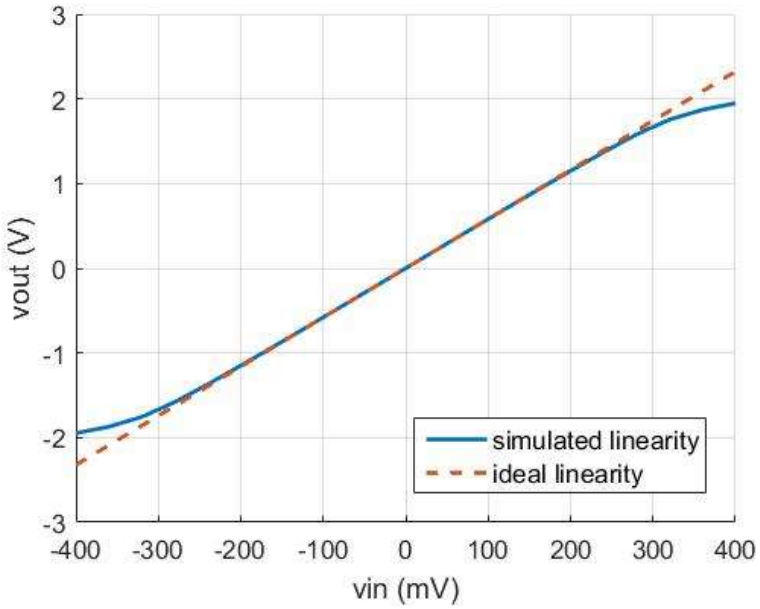
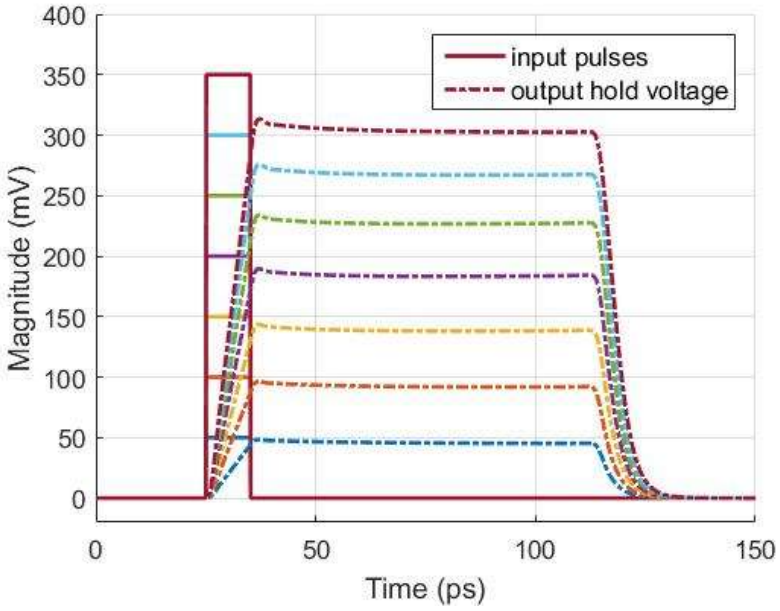


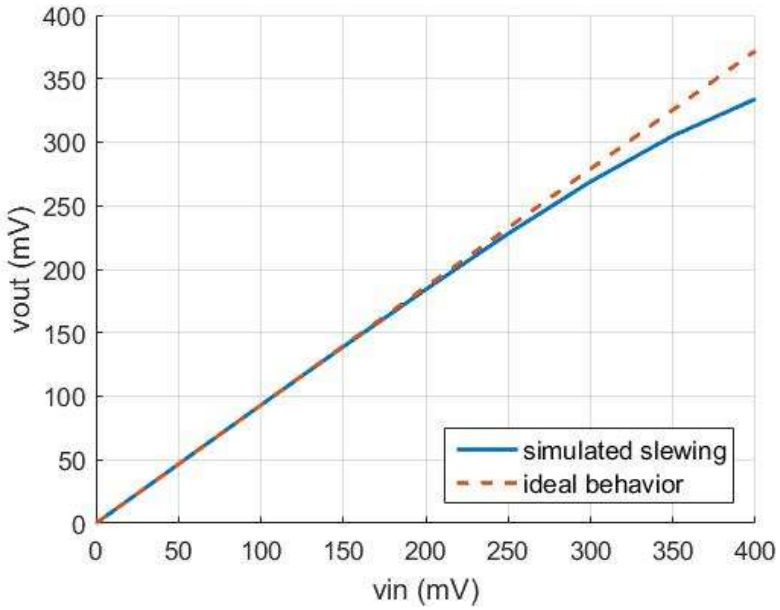
Figure 5-22: *DC linearity of the integrator.*

Figure 5-24 shows the current through C_{INT} for differenent delays T_i at constant pulse amplitude and the corresponding non-ideal current pulses. The current shapes resemble gaussian pulses. The width of the current pulses are larger than the differential delay values showing that due to the bandwidth limitation of the subtractor and integrator the effective pulse width of the IHC lies between 4 to 5.5ps

Table 5-1 shows the comparison of 3dB bandwidth of an ideal rectangular pulse with pulse width T_i and the simulated pulse width of the current in the integration capacitance. Even if the delay T_i generated by the delay element is extremely small, the simulated effective



(a)



(b)

Figure 5-23: *(a) Input pulse amplitude and output hold voltage vs. time. (b) Ratio of output hold voltage vs. input pulse amplitude*

pulse width due to the non-ideal pulse shape limits the bandwidth. To some extent, the bandwidth can be extended by means of bandwidth peaking in the input signal buffer.

Figure 5-25 shows the output of the integrator and the IHC for different T_i. The rise time of the hold signal is longer if T_i is larger. In the IHC a differential amplifier is used to amplify the integrator output signal to achieve sufficient IHC gain.

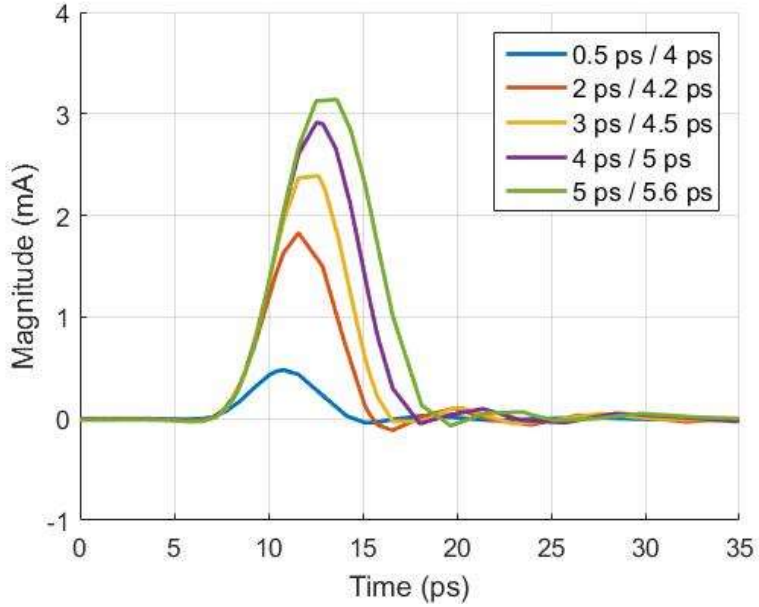


Figure 5-24: *Current through integration capacitance C_{INT} for varied differential delays T_i.*

Table 5-1: *3dB bandwidth f_{3dB_id} of ideal rectangular pulse T_i vs. effective pulse width and 3dB bandwidth f_{3dB_nonid} of simulated current pulse.*

T_i	f_{3dB_id}	Sim. pulse width	f_{3dB_nonid}
0.5 ps	884 GHz	4 ps	77.35 GHz
2 ps	221 GHz	4.2 ps	73.7 GHz
3 ps	147.3 GHz	4.5 ps	68.8 GHz
4 ps	110.5 GHz	5 ps	61.9 GHz
5 ps	88.4 GHz	5.6 ps	55.25 GHz

5.4.5 Power Dissipation

The DC supply voltage is -4.8 V, while the DC current is 230 mA, yields the power consumption of 1100 mW. The power dissipation breakdown chart is shown in Figure 5-26. The high power consumption is due to several reasons. The first reason is that there are some duplicated components like CML switches and delay elements while generally bipolar CML is power hungry. The second reason is that higher current through a differential amplifier was needed to achieve higher linearity and bandwidth. One more reason is that more voltage is needed between VCC and VEE to design differential cascoded amplifier with emitter degeneration, which also brings more linearity and bandwidth. Therefore the supply voltage -4.8 V is pretty large.

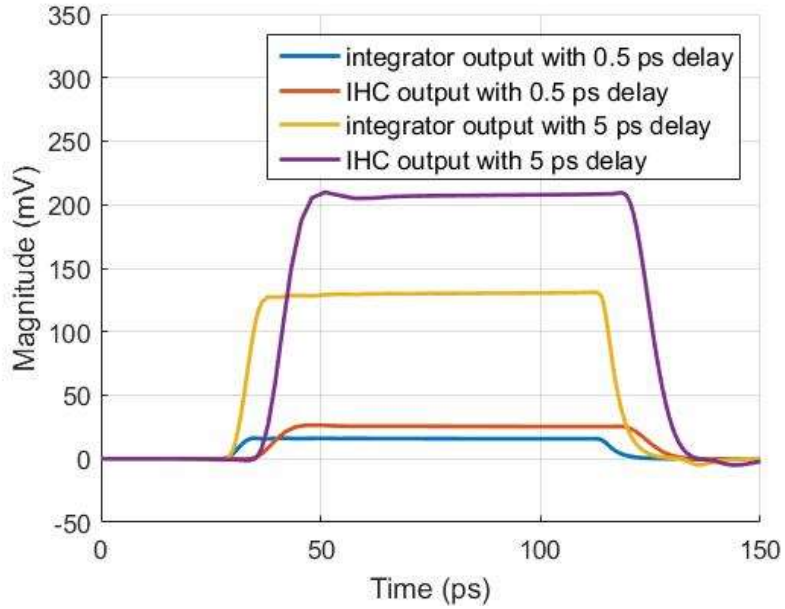


Figure 5-25: *Simulated output signal of the integrator and the IHC for different delays T_i.*

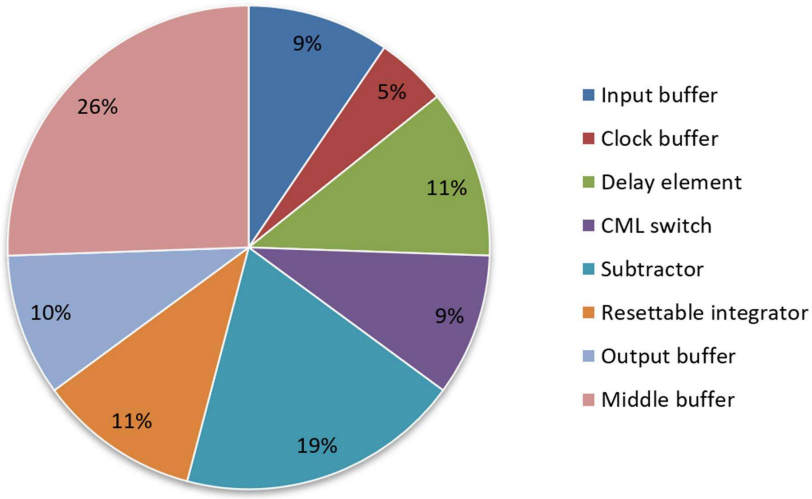


Figure 5-26: *Power consumption breakdown chart.*

5.4.6 Layout and Chip

Figure 5-27 shows the layout of the STI IHC core with buffers. The main components of the design are marked in the Figure. Special care was taken to design all differential high-speed circuitry perfectly symmetric and as compact as possible. The active area is only 320 x 210 um. The chip draws 230 mA from a -4.8 V supply voltage, dissipating 1100 mW.

The chip is fabricated in a 130 nm SiGe BiCMOS technology from IHP (SG13G2) featuring high-speed Silicon Germanium heterobipolar transistors with cut-off frequencies of f_T/f_{max} = 300/500 GHz [40]. Figure 5-28 shows the micro-photograph of the chip. The chip size is 0.9 mm^2. The GSGSG pads at the lower side are used for probing the input

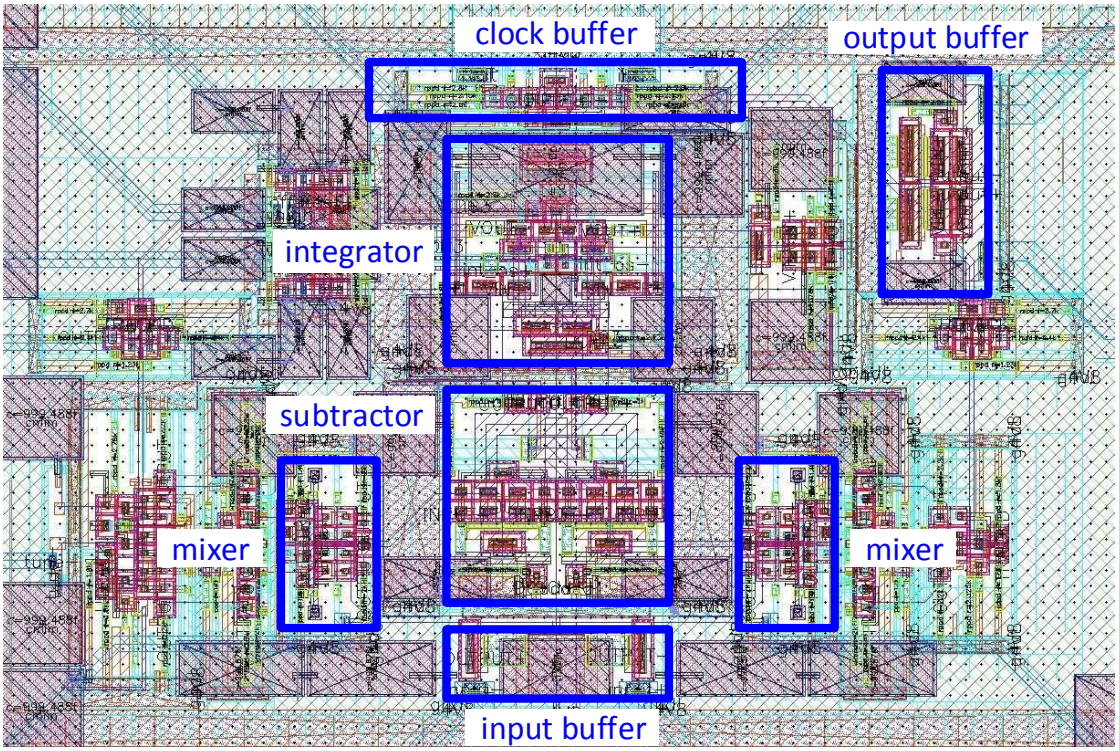


Figure 5-27: *Layout of STI IHC core with buffers.*

signal, while the GSSG pads on the upper and right sides are for the clock and output signals, respectively. The on-chip microstrip transmission lines are separated by a distance of at least 3 times of the signal line width to achieve minimum coupling between them. The DC pads of the chip are located at the chip corners and the left side.

5.5 Measurement Results

The test setup for the IHA is the same as illustrated in Chapter 4. Figure 4-10 is the test setup for transient measurement and spectrum measurement. The main test equipment in this setup are the signal generator 1 (SG1, Keysight E8257D), the PLLs (Linear DC1795A [41], TI LMX2594EVM [42]), the spectrum analyzer (Anritsu MS2760A), and the sampling oscilloscope (Keysight 86100D DCA-X). The signal generator and the PLLs are synchronized to each other. SG1 is used to generate the input signal for the device under test (DUT, IHC). The output of the PLLs provides low phase noise programmable high-frequency clock for both sampling clock of the DUT and the trigger clock of the sampling oscilloscope. The sampling oscilloscope digitizes the output of the DUT. The spectrum analyze the transient signals in the frequency domain.

5.5.1 RF Module

The RF module is shown in Figure 5-29. The PCB is made from an Isola Tera substrate which was mounted onto a copper plate. The chip was placed into a cavity in the substrate

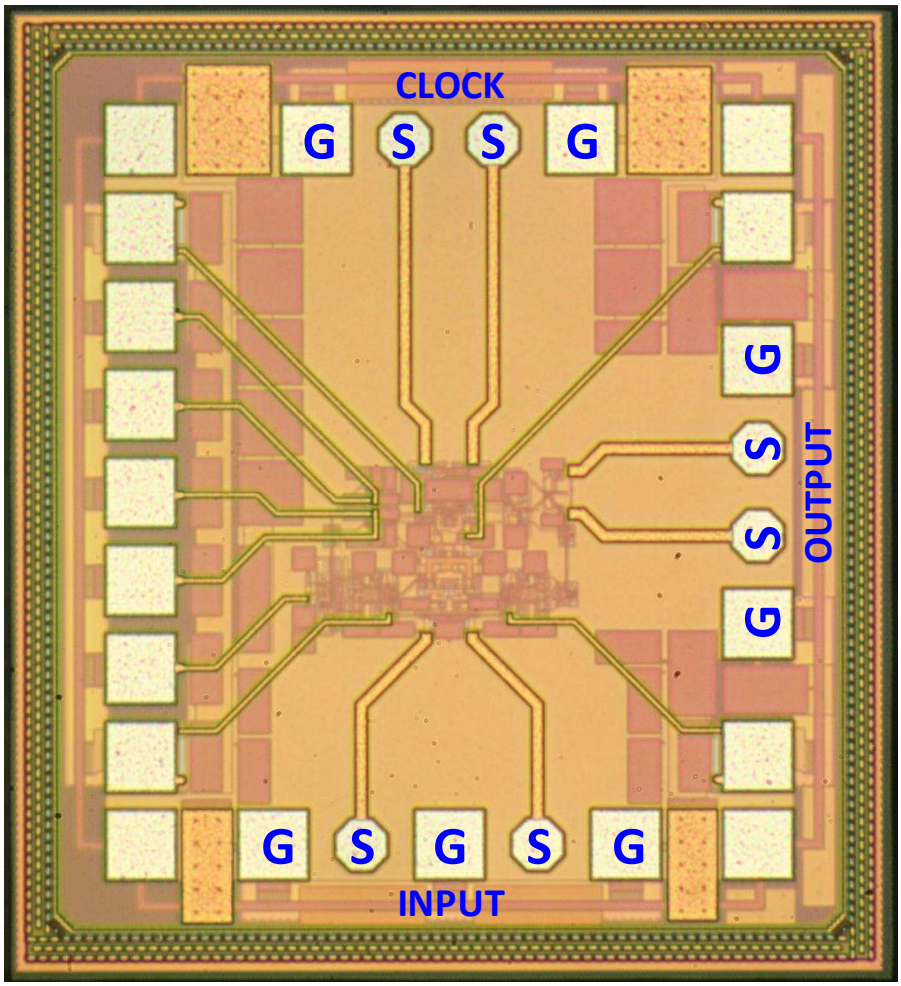


Figure 5-28: *STI IHC chip micro-photograph.*

to keep the bond wires between chip and substrate as short as possible. The positive clock signal was wire-bonded to a microstrip transmission line while the negative clock signal was left open. All RF inputs, outputs and clock signals are terminated on-chip with 50 Ω. The differential output signal was wire bonded to microstrip transmission lines. The RF inputs were not bonded to allow for on-chip probing.

5.5.2 S-Parameter Measurement

The chip was first tested with a broadband vector signal analyzer (VNA, Anritsu VNA MS4647b) to measure the small signal performance for S11 of the input. Figure 5-30 shows the single-ended measurement results from 1 to 70 GHz with the range of -33 dB to -7 dB. One of the differential ports was open, therefore only single-ended measurement was performed.

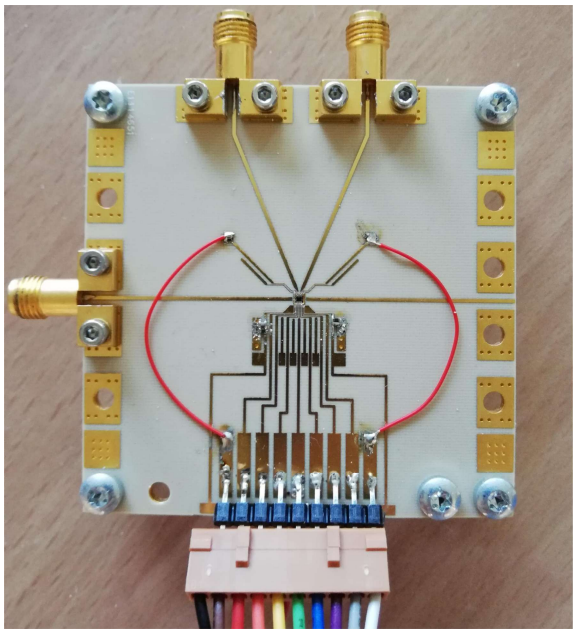


Figure 5-29: *RF module.*

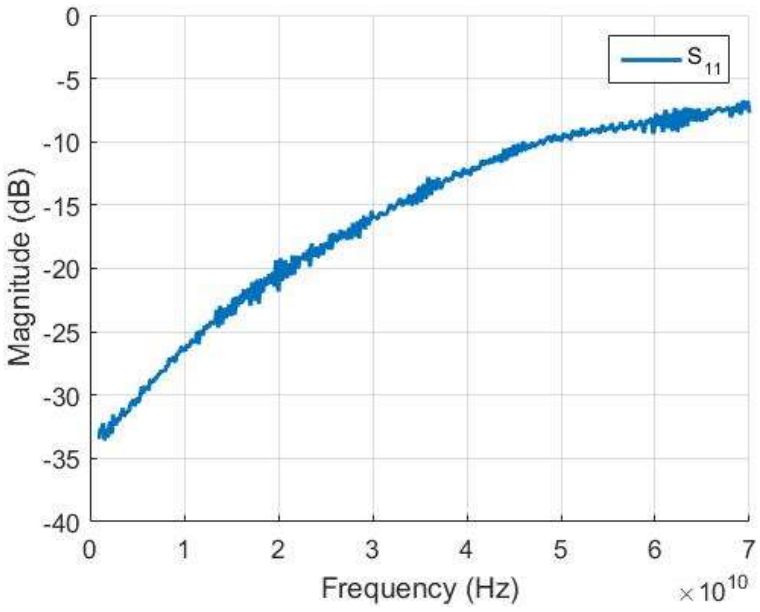
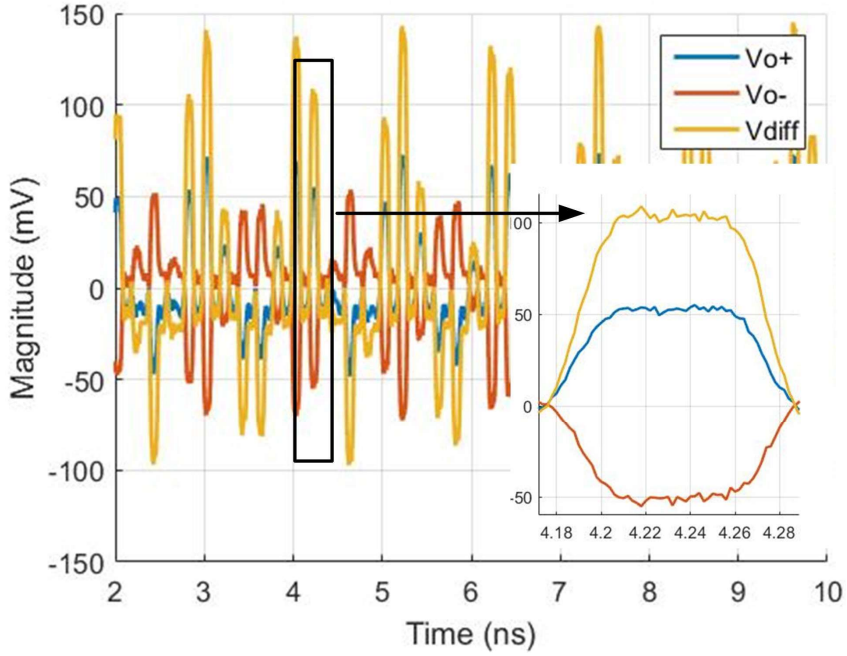


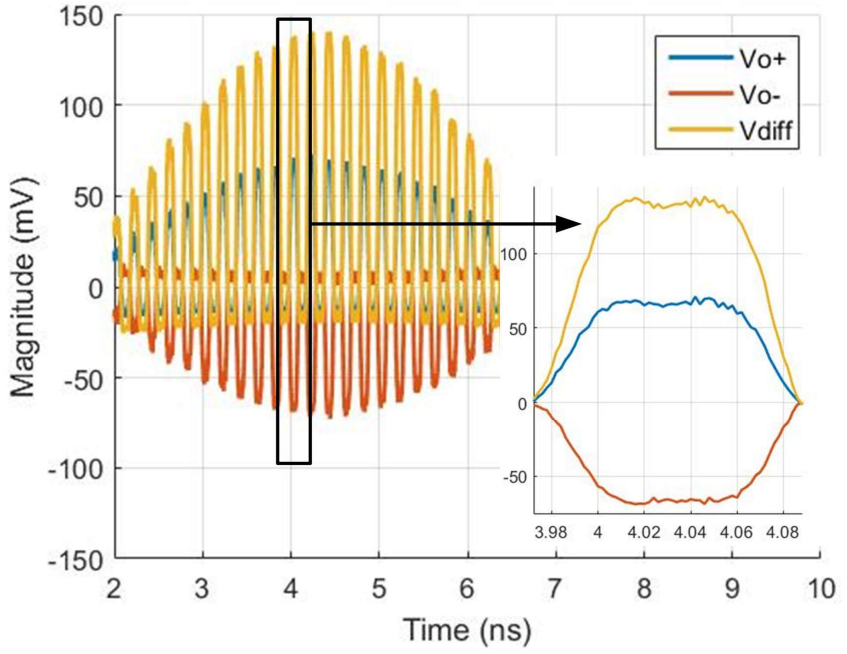
Figure 5-30: *S-parameter measurement result of the input port.*

5.5.3 Transient and Spectrum Measurement

For the time-domain measurement, the input GSGSG pads on chip are contacted with Infinity probes, the output and clock signal are wire-bonded to the RF PCB (Isola Tera substrate) with GSSG pads. The chip was measured with a sampling oscilloscope and a spectrum analyzer. In order to see a very clear hold signal, the sampling rate is limited to 5 GS/s. This topology makes it possible to tune the bandwidth. In our measurements the bandwidth is tuned to be 70 GHz. The chip was tested from 1 to 70 GHz.



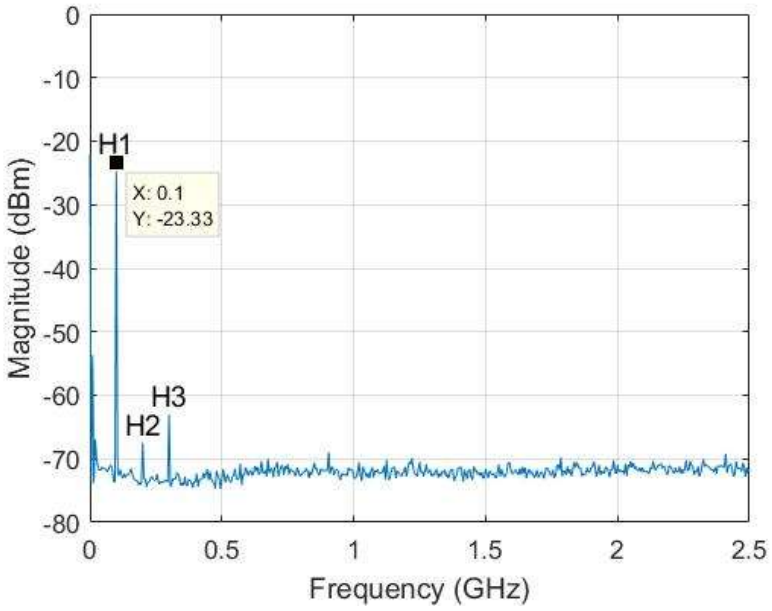
(a)



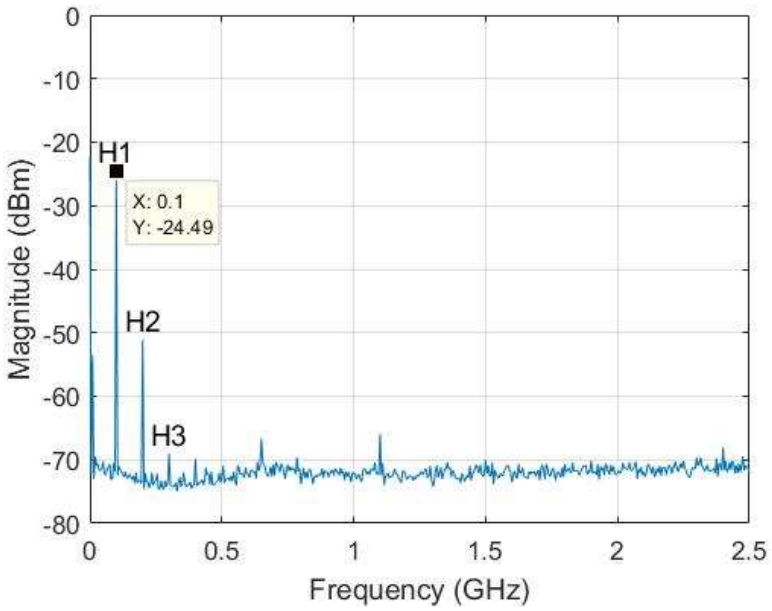
(b)

Figure 5-31: *Measured differential output signal of (a) 0.9 GHz (b) 69.9 GHz 350 mVpp single-ended input sampled by 5 GS/s clock.*

Figure 5-31 shows the single-ended 350 mVpp input signal with the frequency of 0.9 GHz and 69.9 GHz sampled by 5 GS/s clock. Figure 5-31 shows the positive and negative output signals from the oscilloscope. The hold-mode signal gives excellent performance with reference to feedthrough, droop and so on. The differential output is calculated with



(a)

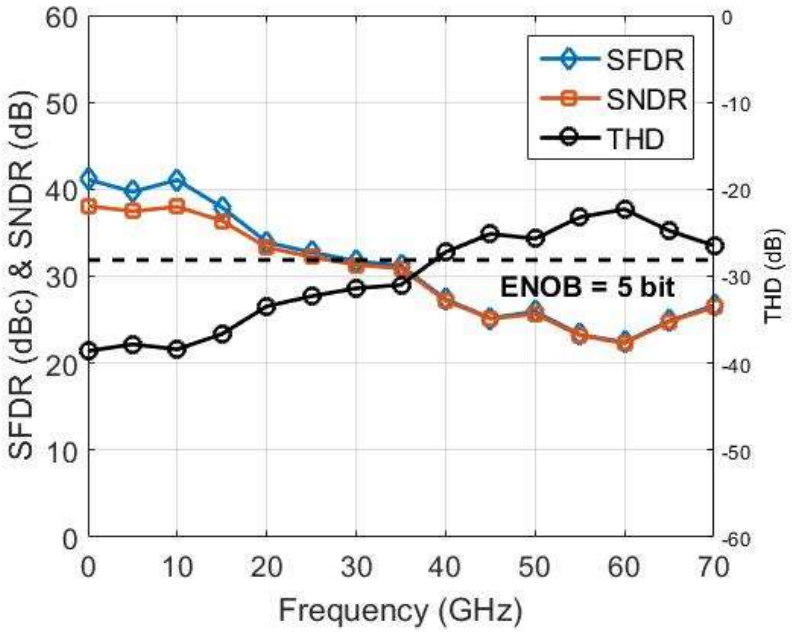


(b)

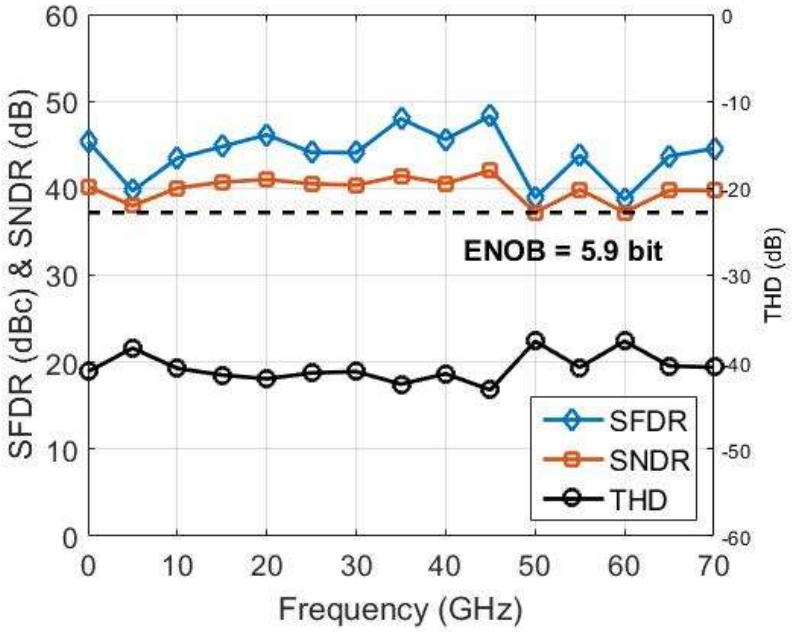
Figure 5-32: *Spectrum of single-ended output signal of (a) 4.9 GHz (b) 69.9 GHz single-ended 350 mVpp input sampled by 5 GS/s clock.*

MATLAB.

The single-ended output of 4.9 GHz and 69.9 GHz singled-ended 350 mVpp input sampled at 5 GS/s are measured with the spectrum analyzer shown in Figure 5-32. The frequency span is the corresponding Nyquist zone of 2.5 GHz, the resolution bandwidth of the spectrum analyzer is set to 10 kHz. The sampled fundamental signals at 0.1 GHz for two input frequencies show that the large-signal 1dB bandwidth of the STI IHC is 70 GHz. The lower peak amplitude in the spectrum is due to the reset phase at the output



(a)



(b)

Figure 5-33: *SFDR, THD vs. input frequency by 5 GS/s clock with (a) even and odd order harmonics (b) only odd order harmonics.*

signal.

Figure 5-33 is the SFDR, SNDR and THD vs. frequency by 5 GS/s clock with and without even order harmonics. The THD is dominated by the 2nd order harmonics at high frequency. The best case THD is -39 dB while SFDR is 41 dBc and SNDR-related ENOB is 6 bit. However if an ideal differential input can be realized, it results to Figure 5-33(b). The THD is at least to -38 dB and SFDR to 39 dBc with ENOB >5.9 bit from DC to 70 GHz. Therefore Figure 5-33 can be understood as the worst and best case of the

STI IHC.

5.6 Conclusion

This chapter presents an STI sampler using 130 nm SiGe BiCMOS technology. A novel diff-delay scheme for the STI samplers is proposed. The STI IHC is analyzed with the aspects of droop, bandwidth, noise and jitter. The preliminary consideration of negative resistance with cross-coupled transistors is discussed. The measured 1dB large-signal bandwidth of the STI sampler is around 70 GHz. Sampling the input signal at 5 GS/s yields a peak ENOB of 6 bit at 9.9 GHz. The comparison of this chip to the state of the art of sampling circuits is shown in Table 5-2. Our STI sampler shows the largest large-signal bandwidth compared to all other samplers published so far. The low sampling rate is chosen to clearly show the clean and stable hold-mode performance. With the proposed STI IHC topology excellent performance with respect to bandwidth and signal integrity is achieved. A drawback of the circuit is the high power dissipation and lower sampling rate compared to conventional THAs.

Table 5-2: *Comparison to the state of the art.*

	[31]	[32]	[27]	[A1]	[A2]	[A3]
Architecture	SEF	Switched capacitor	Charge sampling	SEF	SEF	Charge sampling
Input amplitude	160 mVpp	800 mVpp	500 mVpp	450 mVpp	450 mVpp	350 mVpp
Max. sampling rate	108 GS/s	25 GS/s	25.6 GS/s	40 GS/s	10 GS/s	5 GS/s
Small-signal BW	40 GHz (3dB)	70 GHz (3dB)	N/A	70 GHz (3dB)	65 GHz (3dB)	N/A
Large-signal BW	N/A	55 GHz (3dB)	40 GHz (1dB)	19 GHz (3dB)	61 GHz (3dB)	70 GHz (1dB)
THD@f_{in}	-49dB@1GHz	-39dB@21GHz	-44dB@1GHz	-47dB@1GHz	-44dB@29GHz	-39dB@9.9GHz
ENOB@f_{in}	N/A	4.9@3GHz	6.4@1GHz	7.5@1GHz	7@29GHz	6@9.9GHz
Power	87 mW	73 mW	913 mW	440 mW	375 mW	1100 mW
FoMw	N/A	98 fJ/conv.-step	422 fJ/conv.-step	61 fJ/conv.-step	293 fJ/conv.-step	3438 fJ/conv.-step
FoMs	N/A	150 dB	147 dB	153 dB	156 dB	146 dB
Die area	0.49 mm^2	0.53 mm^2	1.5 mm^2	0.79 mm^2	0.72 mm^2	0.9 mm^2
Process	55 nm SiGe BiCMOS	28 nm CMOS	130 nm SiGe BiCMOS	130 nm SiGe BiCMOS	130 nm SiGe BiCMOS	130 nm SiGe BiCMOS

6 Conclusion and Outlook

In this thesis, I investigated on sampling techniques for TI ADCs. One of the challenges of designing a TI ADC is that the bandwidth of the system is limited by the sampler while the sampling rate is guaranteed by the interleaving topology. Therefore the sampler bandwidth is the first priority of our design.

We categorize the sampling techniques into two types, TH sampling technology and STI sampling technology. There are several circuit topologies for the TH sampling, including switched-capacitor, diode-bridge and SEF. These are conventional ways to implement the sampler in an ADC system. With the development of circuit and fabrication technology, these conventional techniques are able to offer large bandwidth of over 50 GHz. As an alternative to TH sampling, it is possible to use an STI IHC to use charge sampling for an ultra-broadband electronic sampling system. Multiple sampler characteristics including bandwidth, sampling jitter, noise and droop are discussed and analyzed mathematically for TH sampling and STI sampling.

The measurement techniques for samplers are basically covered by three measurements, s-parameter measurement, transient measurement and spectrum measurement. S-parameter measurement checks the circuit in frequency domain, usually the S11 for signal ports and S21 from output port to input port are measured. The transient and spectrum measurement are both done in time domain. The spectrum measurement applies spectrum analysis on the transient output signal of the sampler.

We present three circuit topologies, two of them use SEF TH sampling [A1][A2] and the last one uses charge sampling with STI IHC [A3]. The design methodology on the system and circuit levels is discussed. Three ICs are designed and fabricated with IHP SiGe BiCMOS 130 nm technology. Tabel 5-2 shows the comparison between our chips and state-of-the-art.

The first design is an input-buffer-less SEF THA [A1]. Often the THA small-signal bandwidth is limited by the input buffer, a differential amplifier. Therefore this design removes the differential amplifier and uses SEF directly as the input buffer. The issue is that the pull-down resistor is fixed to 50 Ω, therefore large pull-down current is needed to switch the sampler from track mode to hold mode. Inductive peaking technique is applied to further increase the bandwidth for higher frequency range. This chip shows the best sampling rate of 40 GS/s, small-signal bandwidth of 70 GHz and the best-case ENOB of 7.5 bits among three chips presented in this thesis. Furthermore, the ENOB of 7.5 bits at 1 GHz is beyond the state-of-the-art. Its drawback is also pretty clear, the large-signal bandwidth much lower than the small-signal bandwidth.

The second design uses an SEF with differential amplifier as buffer, whereby the buffer can be switched off [A2]. When the buffer is switched off, the effect of hold mode is almost perfect even with relative low pull-down current. Capacitive and inductive peaking are both applied to increase the bandwidth. This chip shows ultra-high bandwidth for both small-signal and large-signal measurement, the small-signal bandwidth is measured to be 65 GHz while the large-signal bandwidth is 61 GHz. The ENOB of 7 bits at 34 GHz is also beyond the state-of-the-art. The ENOB is larger than 5 bits for the whole input frequency

range from 0 to 70 GHz. The drawback is the reduced sampling rate and increased supply voltage compared to the first design.

The third design is an STI IHC [A3]. I proposed several architectures of the STI IHC, including single delay element and differential delay elements. Although the differential delay elements consumes more power, this solution offers better sampling performance. The analysis of STI IHC is done mathematically in detail for non-ideal sampling, non-zero rise and fall time, and integration capacitor leakage. This chip shows 70 GHz 1dB large-signal bandwidth, which is the highest bandwidth compared to any sampler in silicon technology published so far. It also offers 5.9 bits ENOB in an input frequency range from 0 to 70 GHz when even order harmonics are excluded. The drawback is however the low sampling rate because more clock states are required to operate an IHC.

The SEF THA as a traditional technology is widely used in different applications, it still shows outstanding performance with modern silicon technology. The bandwidth limitation of the SEF THA is very clear, 60 GHz 3dB bandwidth reaches almost the limit with current technology.

The charge sampling technology using STI IHC needs more design effort because of its more complicated architecture. However it exhibits the great advantage of extending the bandwidth of a sampler. This technology is a good candidate when designing an ultra-broadband TI ADC. The non-ideal pulse shape generated by the circuit components becomes the bottleneck of the theoretical infinite bandwidth. The sampling rate could be the biggest issue which might limit the application of this technology.

In the future research, more design effort should be given to improve the sampling rate and reduce the power consumption of both SEF THA and STI IHC. Especially for a TI ADC these two design goals are very critical. Another easily overlooked point of ultra-broadband sampler design is the sampling jitter. The larger the bandwidth, the more influence the chip gets from the jittery sampling clock. One solution is to use the optical PLL or optical signal directly as clock [10][11][12]. It is a very interesting topic to build these samplers with multiple TI channels controlled by an optical clock source.

Publications by the Author

[A1] Liang Wu, Maxim Weizel, and J. Christoph Scheytt. “A 70 GHz Small-signal Bandwidth 40 GS/s Track-and-Hold Amplifier in 130 nm SiGe BiCMOS Technology”. In: *2019 26th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*. IEEE, 27.11.2019 - 29.11.2019, pp. 1–4.

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[A3] Liang Wu, Maxim Weizel, and J. Christoph Scheytt. “70 GHz Large-signal Bandwidth Sampler Using Current-mode Integrate-and-Hold Circuit in 130 nm SiGe BiCMOS Technology”. In: *2019 IEEE Asia-Pacific Microwave Conference (APMC)*. IEEE, 10.12.2019 - 13.12.2019, pp. 1697–1699.

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Das Heinz Nixdorf Institut – Interdisziplinäres Forschungszentrum für Informatik und Technik

Das Heinz Nixdorf Institut ist ein Forschungszentrum der Universität Paderborn. Es entstand 1987 aus der Initiative und mit Förderung von Heinz Nixdorf. Damit wollte er Ingenieurwissenschaften und Informatik zusammenführen, um wesentliche Impulse für neue Produkte und Dienstleistungen zu erzeugen. Dies schließt auch die Wechselwirkungen mit dem gesellschaftlichen Umfeld ein.

Die Forschungsarbeit orientiert sich an dem Programm „Dynamik, Mobilität, Vernetzung: Eine neue Schule des Entwurfs der technischen Systeme von morgen“. In der Lehre engagiert sich das Heinz Nixdorf Institut in Studiengängen der Informatik, der Ingenieurwissenschaften und der Wirtschaftswissenschaften.

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The Heinz Nixdorf Institute is a research centre within the Paderborn University. It was founded in 1987 initiated and supported by Heinz Nixdorf. By doing so he wanted to create a symbiosis of computer science and engineering in order to provide critical impetus for new products and services. This includes interactions with the social environment.

Our research is aligned with the program “Dynamics, Mobility, Integration: Enroute to the technical systems of tomorrow.” In training and education the Heinz Nixdorf Institute is involved in many programs of study at the Paderborn University. The superior goal in education and training is to communicate competencies that are critical in tomorrows economy.

Today eight Professors and 130 researchers work at the Heinz Nixdorf Institute. Per year approximately 15 young researchers receive a doctorate.

This work investigates ultra-broadband sampling techniques for time-interleaved analog-to-digital converters. The sampling techniques are mathematically analyzed in detail and compared with each other. The mathematical analysis allows to predict multiple sampler characteristics including sampler bandwidth, sampling precision and so on. Two different sampling techniques are studied. The conventional sampling technique is implemented with a track and hold amplifier (THA) using switched emitter follower sampling topology. As an alternative sampling technique the short-time-integration (STI) technique using an integrate-and-hold circuit (IHC) is implemented. Three samples chips (2 THA chips and 1 IHC chip) were fabricated in state-of-the-art 130 nm SiGe BiCMOS technology. The measured results exceed the state of the art in samplers wrt. bandwidth and effective resolution (effective number of bits, ENOB).